EmeraldPools PDB

Project Name :
PCB Number:
PCB REV:
PCBA REV:
LAST UPDATE:

Cover Page

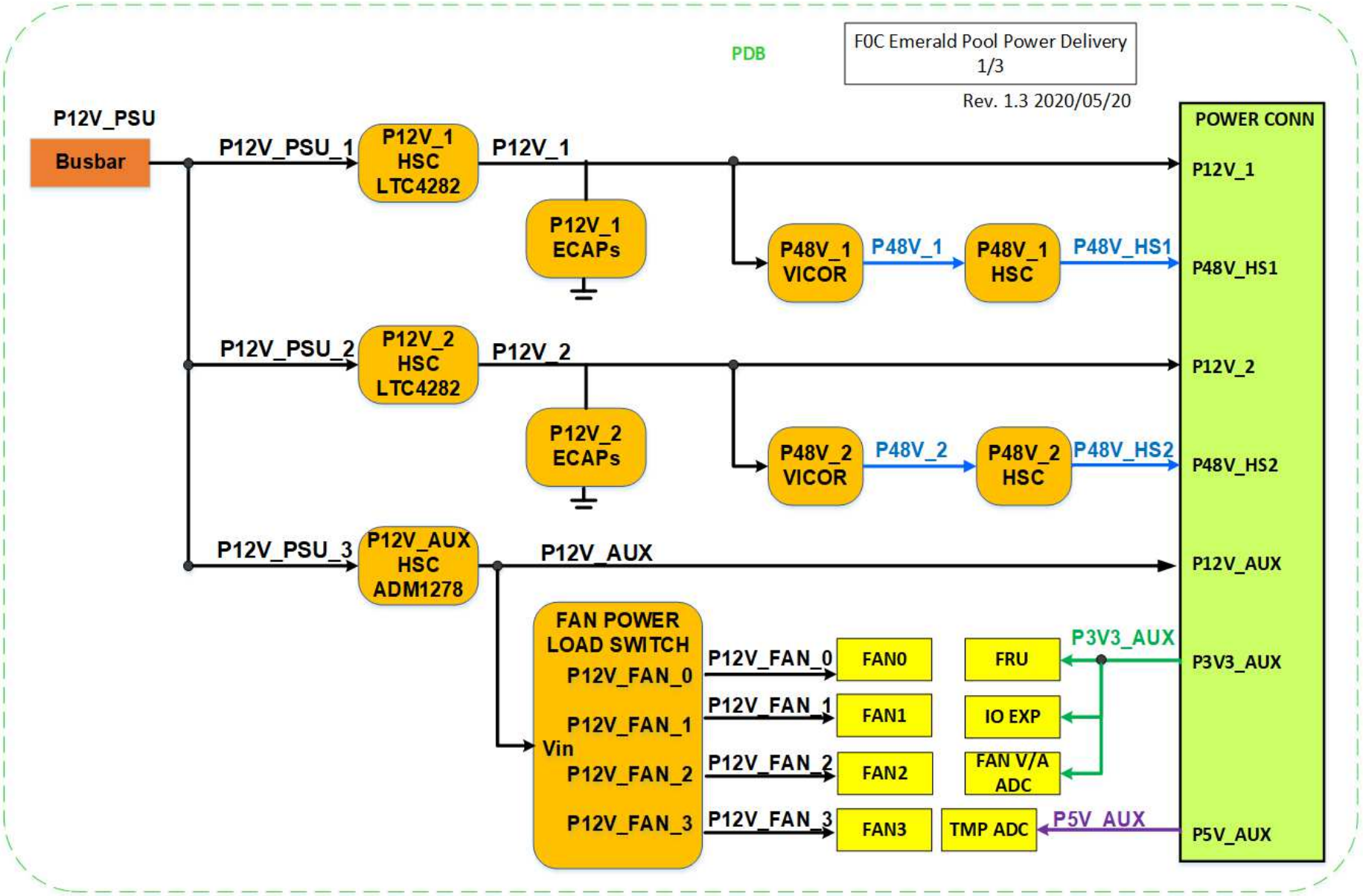
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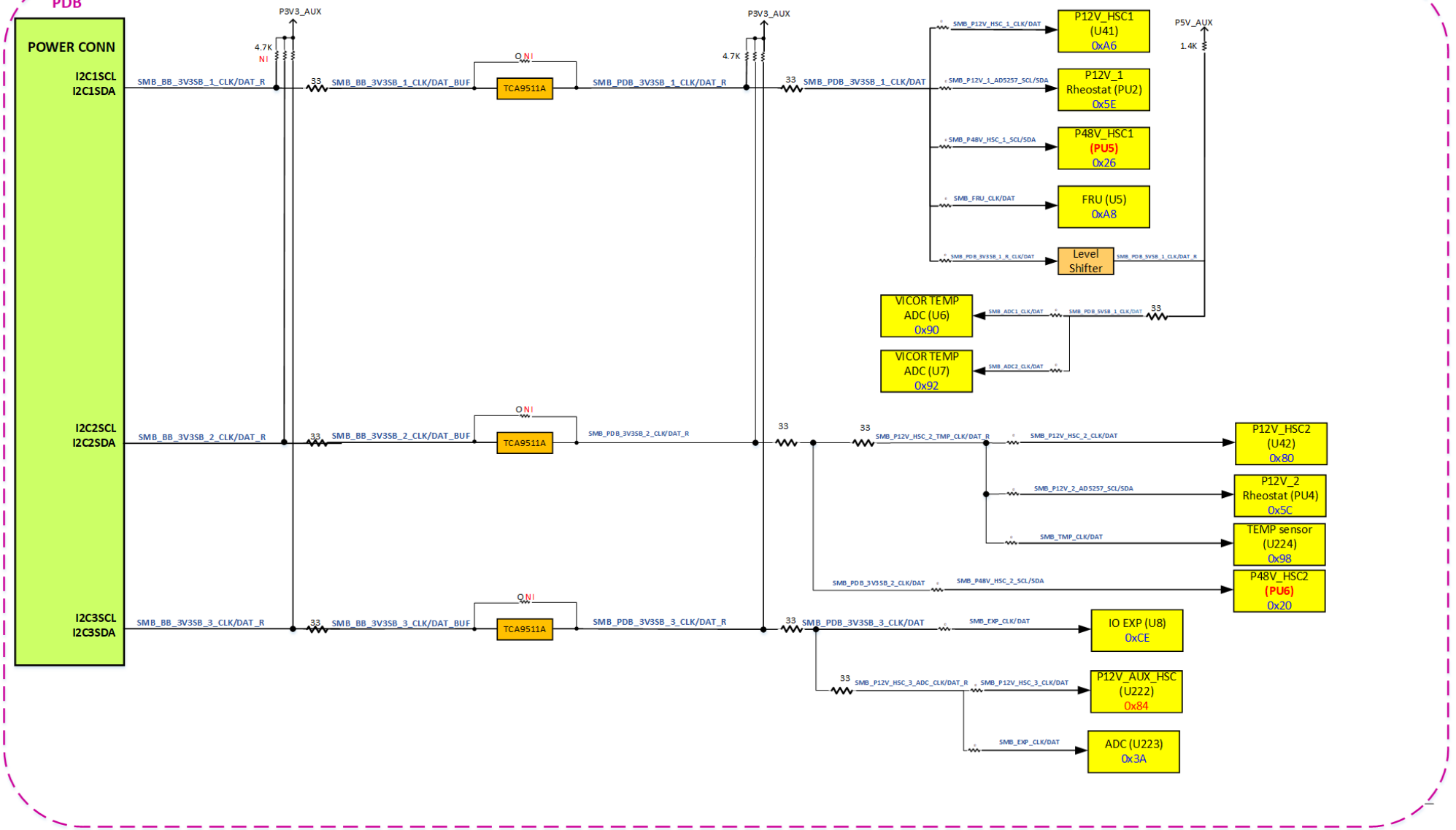
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BOARD BLOCK DIAGRAM

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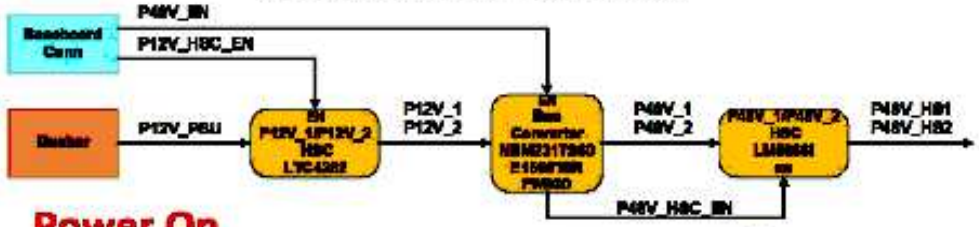
JG7 Emerald Pool SMB
block diagram 2/2
Rev. 1.3 2020/05/14



I2C BLOCK DIAGRAM

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Power On/Off Sequence



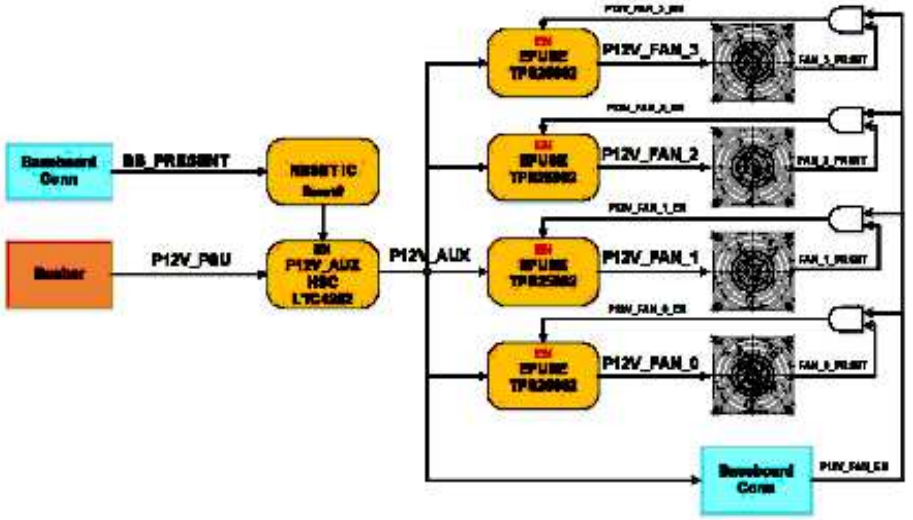
Power On

1. P12V_PSU ON
2. CPLD on BB turn P12V_HSC_EN HIGH
3. Output P12V_1/P12V_2
4. CPLD on BB turn P48V_EN HIGH
5. Output P48V_1/P48V_2
6. Bus Converter PWRGD turn HIGH
7. Output P48V_HS1/P48V_HS2

Power Off

1. P12V_PSU OFF
2. CPLD on BB turn P48V_EN LOW
3. Power off P48V_HS1/P48V_HS2
4. CPLD on BB turn P12V_HSC_EN LOW
5. Power off P12V_1/P12V_2

Power On/Off Sequence



Power On

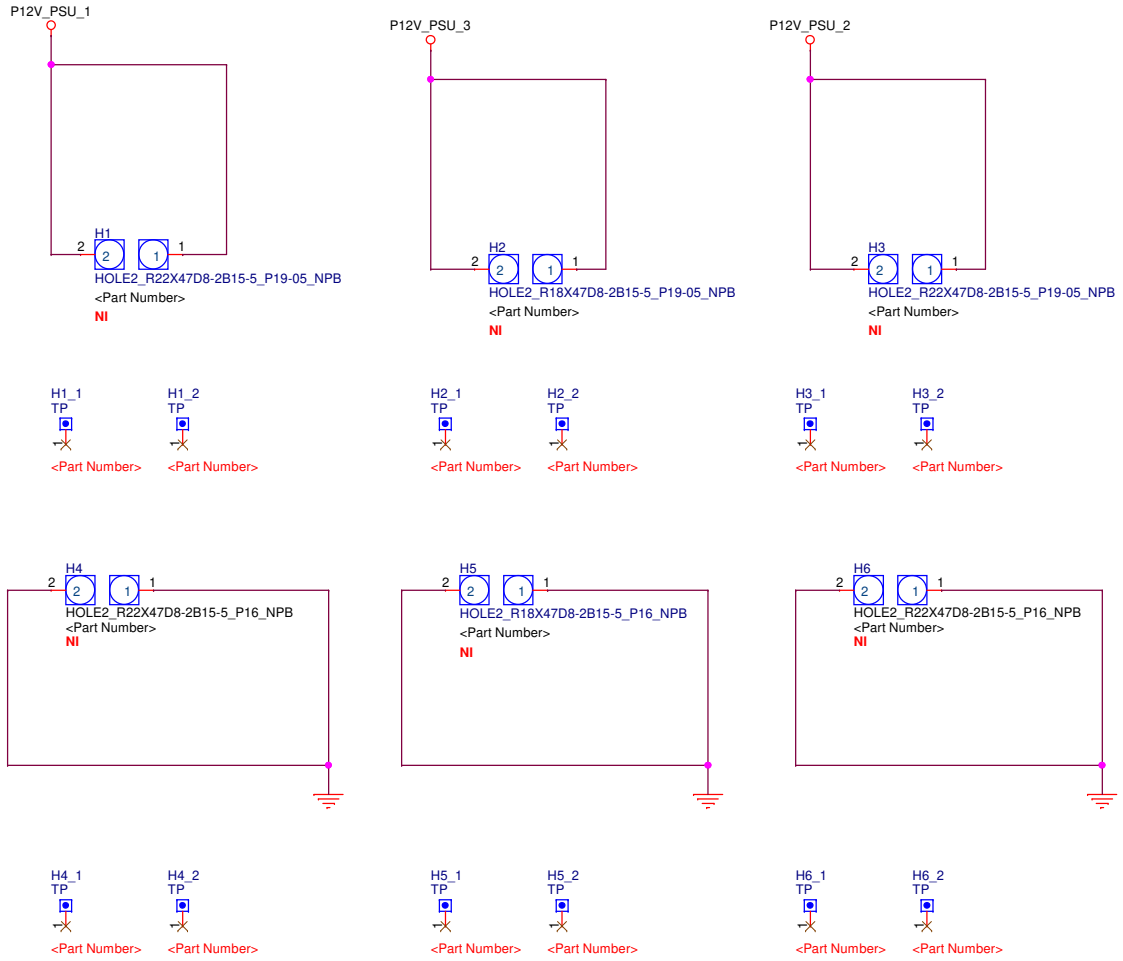
1. P12V_PSU ON
2. BB_PRESENT turn HIGH
3. RESET IC Delay 200 ms to Enable P12V_AUX HSC
4. Output P12V_AUX
5. P12V_FAN_EN turn HIGH
6. Output P12V_FAN

Power Off

1. P12V_PSU OFF
2. BB_PRESENT turn LOW
3. RESET IC Disable P12V_AUX HSC
4. Power off P12V_AUX
5. Power off P12V_FAN

POWER SEQUENCE DIAGRAM

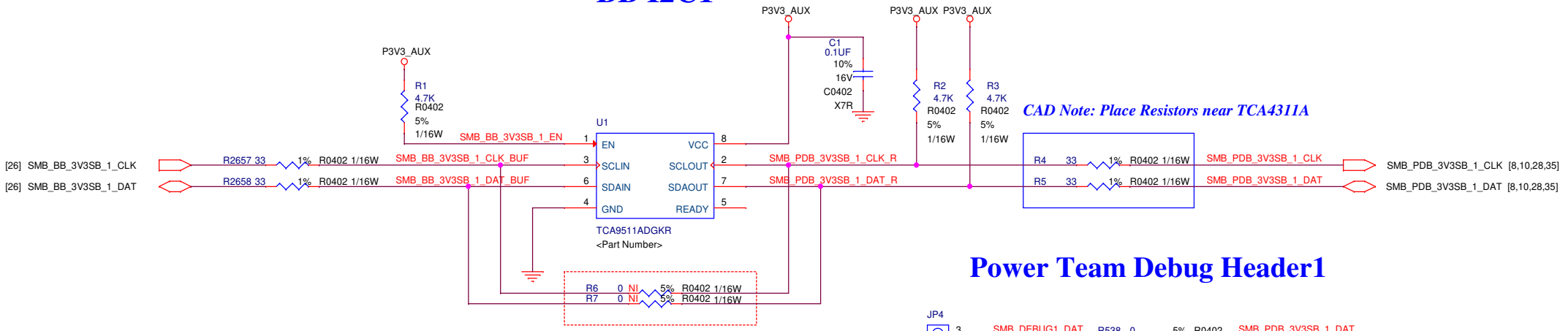
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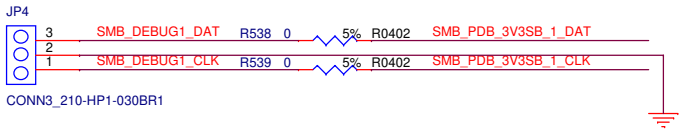
BUS BAR NUT

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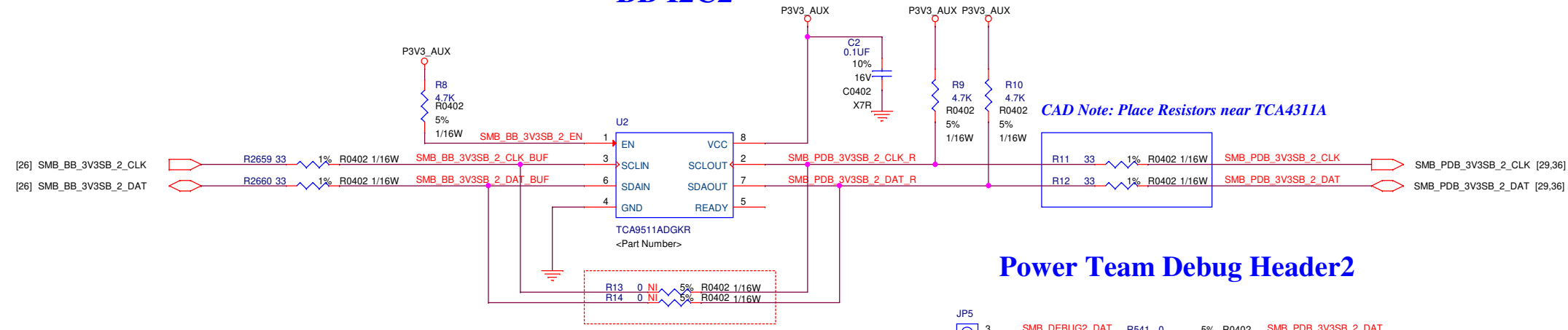
BB I2C1



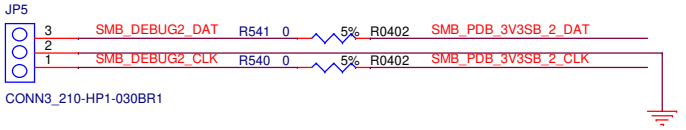
Power Team Debug Header1



BB I2C2



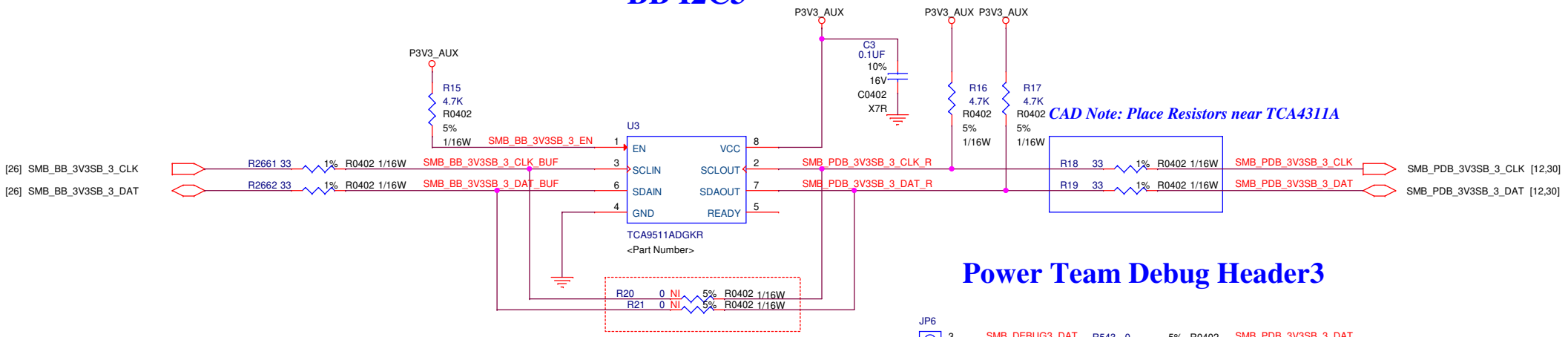
Power Team Debug Header2



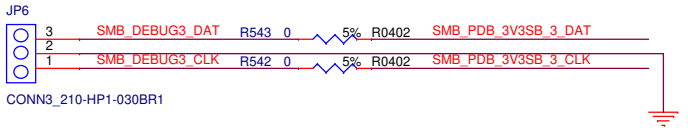
I2C ISOLATION_1

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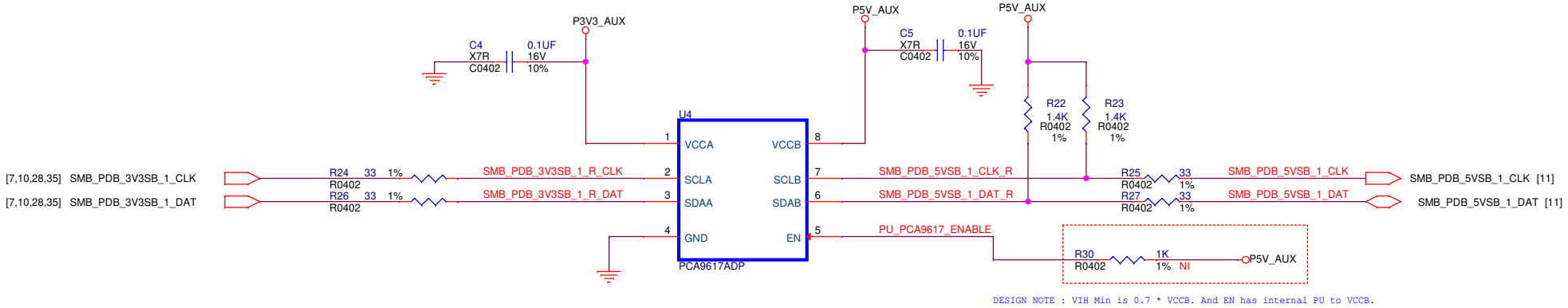
BB I2C3



Power Team Debug Header3



TMP ADC I2C LEVEL SHIFT

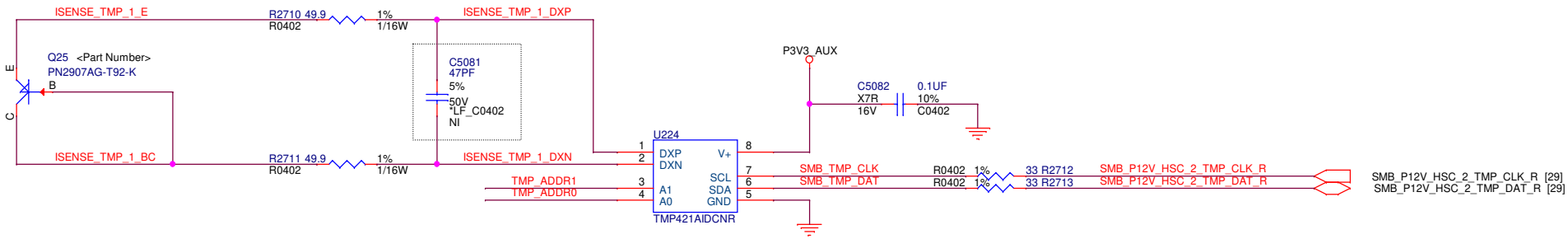


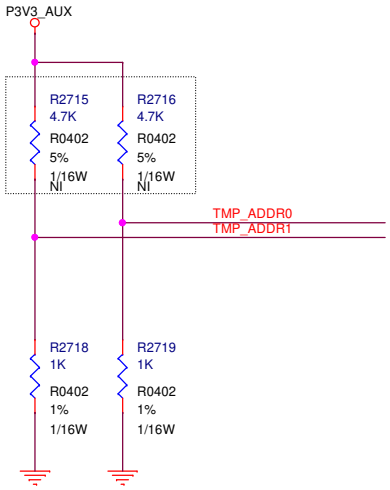
DESIGN NOTE : VIH Min is 0.7 * VCCB. And EN has internal PU to VCCB.

I2C ISOLATION_2

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BOM NOTE : Q25 DIP PART





ADDRESS 0X98

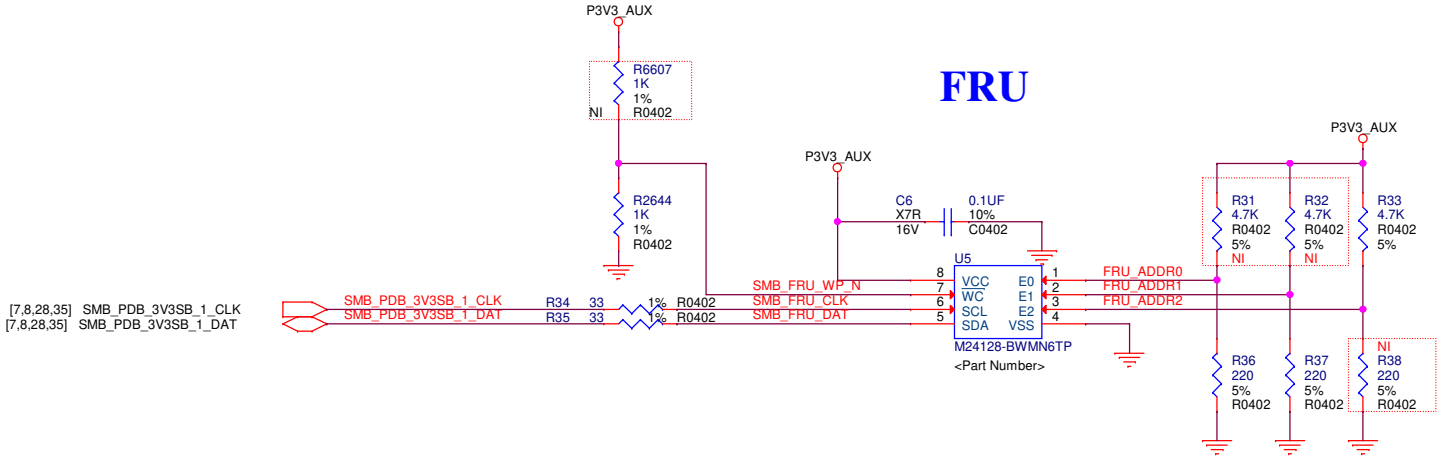
Table 9. TMP421 Slave Address Options

TWO-WIRE SLAVE ADDRESS	A1	A0
1001 100	0	0
1001 101	0	1
1001 110	1	0
1001 111	1	1

TMP SENSOR

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FRU



ADDRESS 0XA8

Table 2. Device Select Code

	Device Type Identifier[1]				Chip Enable Address[2]			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	E2	E1	E0	$\overline{RW}$

Note: 1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

FRU address

VICOR TMP ADC

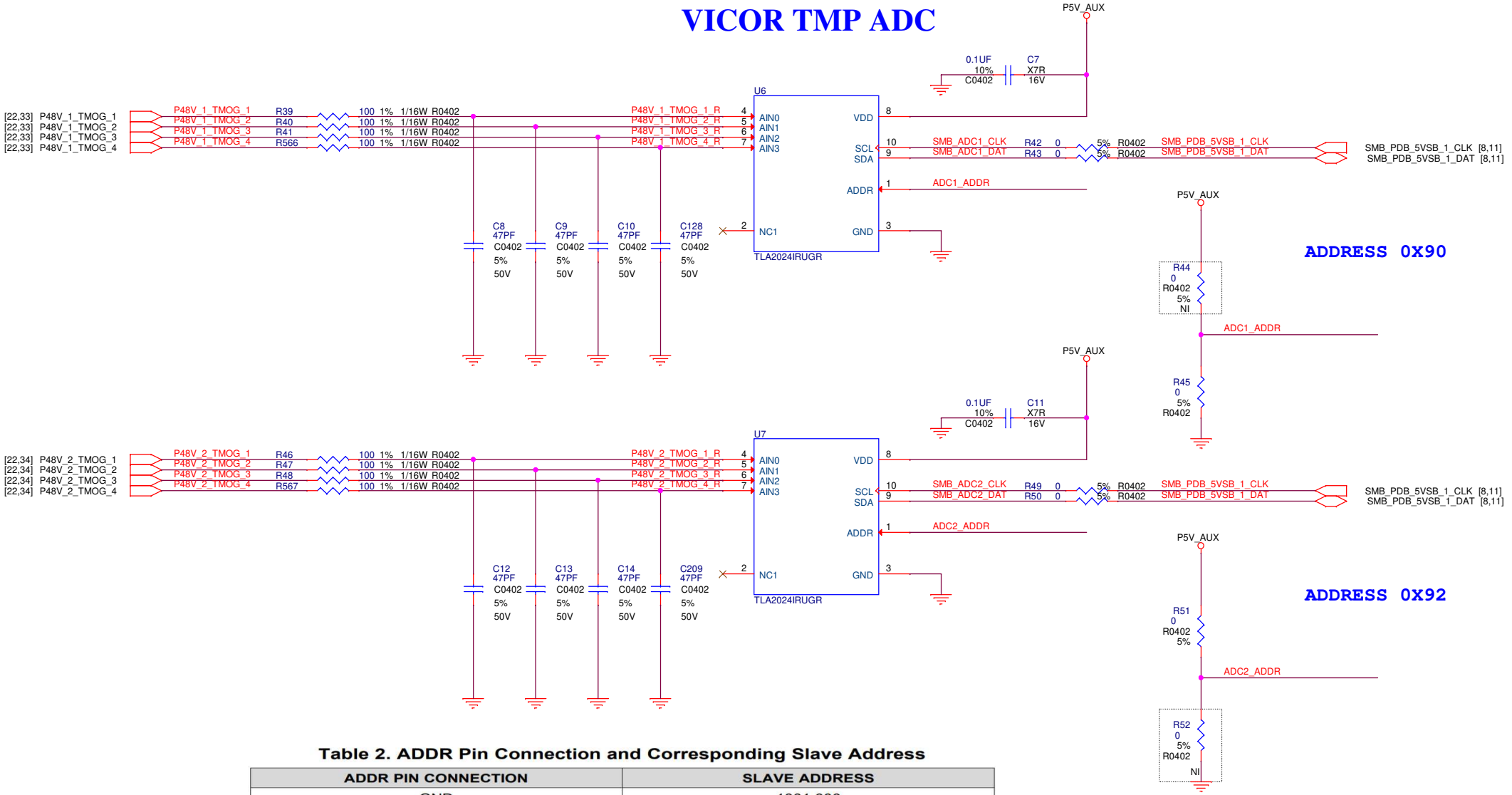
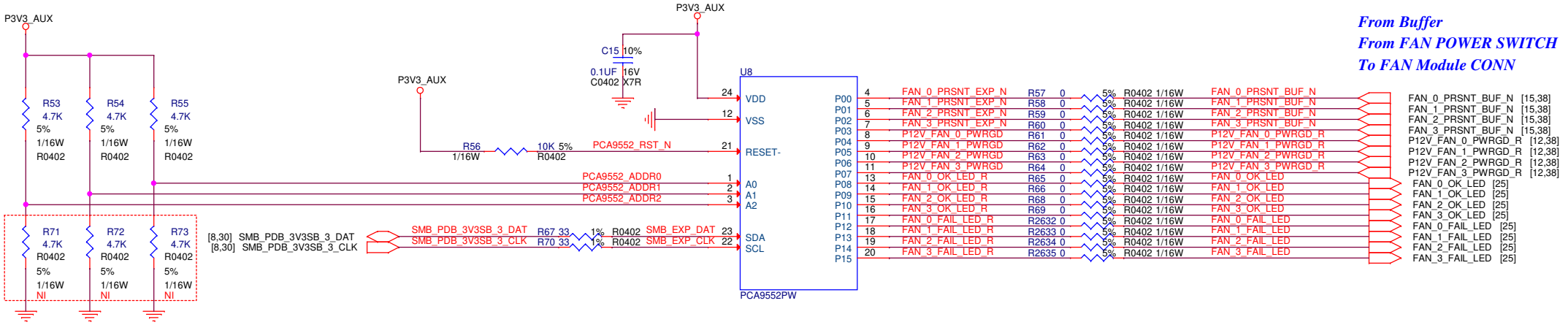


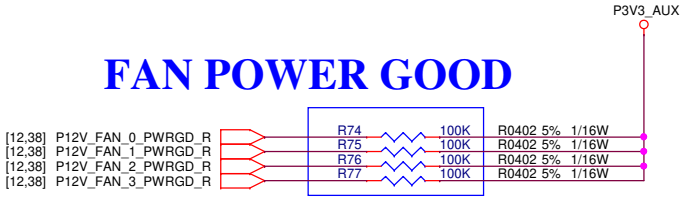
Table 2. ADDR Pin Connection and Corresponding Slave Address

ADDR PIN CONNECTION	SLAVE ADDRESS
GND	1001 000
VDD	1001 001
SCL	1001 011

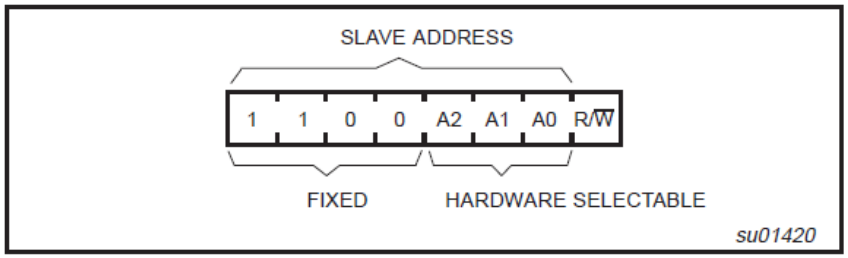


From Buffer
From FAN POWER SWITCH
To FAN Module CONN

FAN POWER GOOD



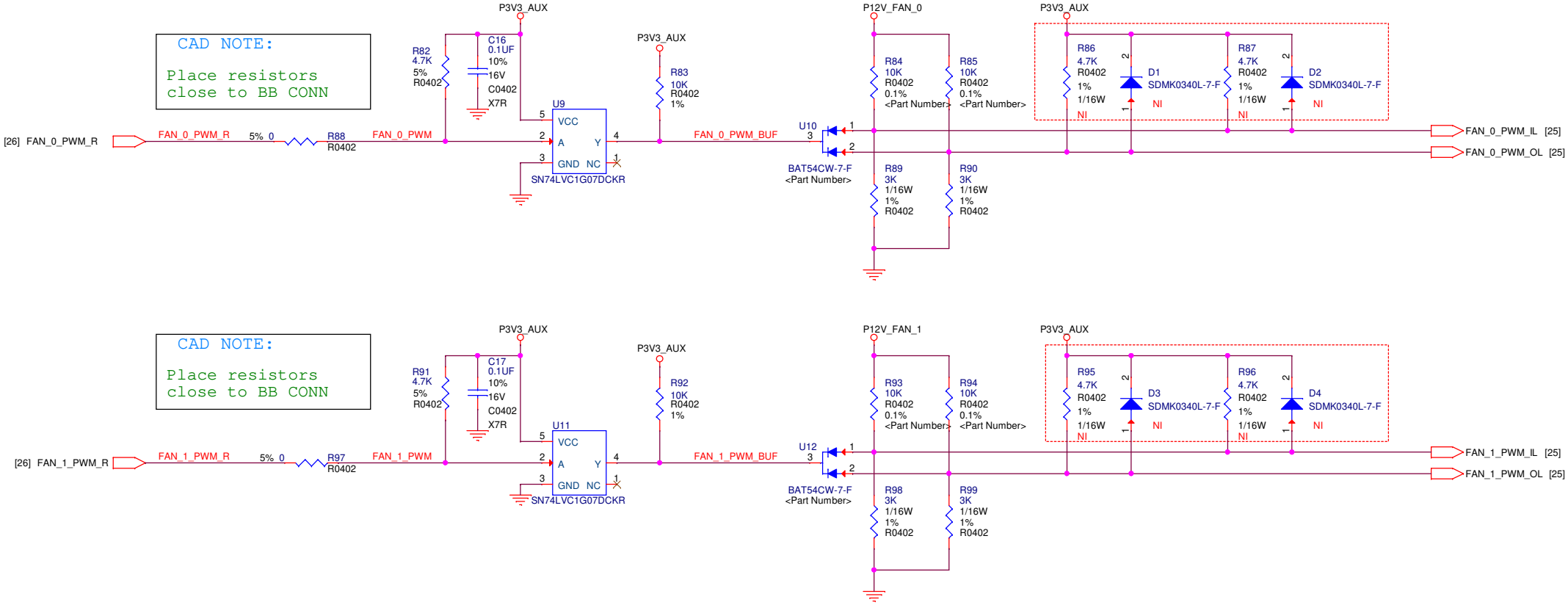
ADDRESS 0XCE



I2C IO EXP

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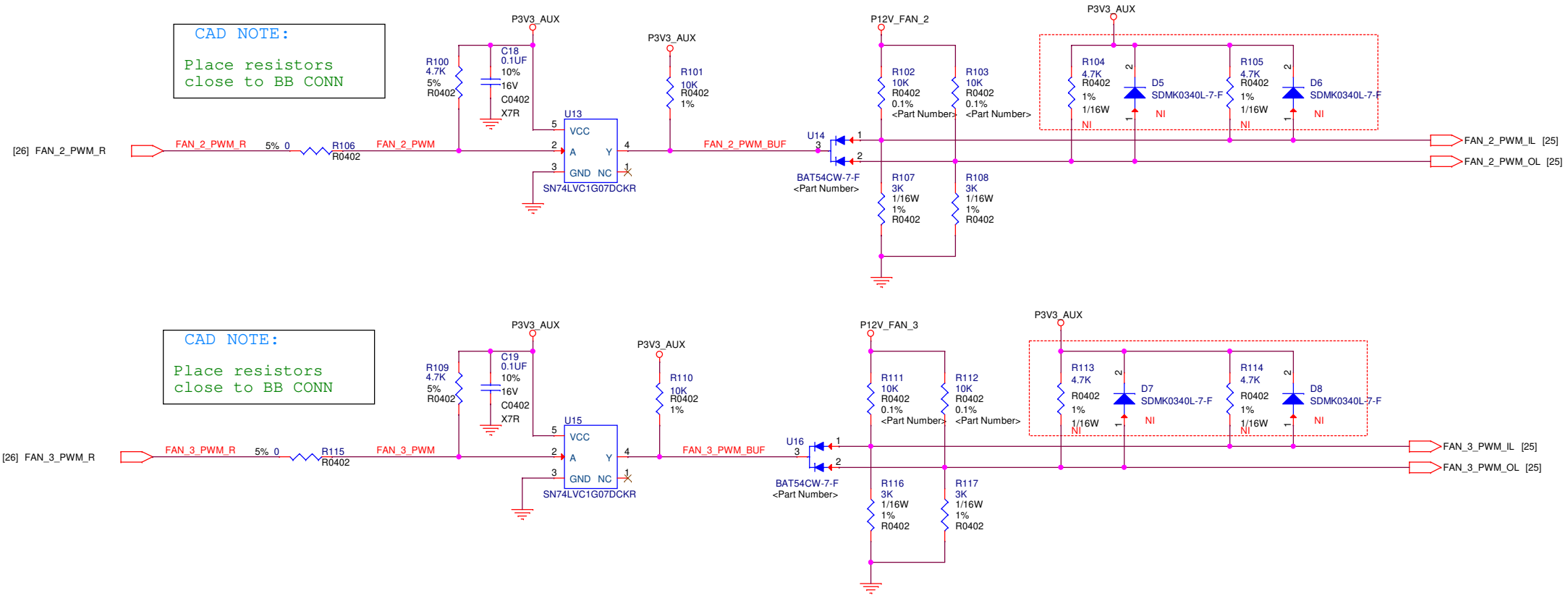
FAN 0&1 PWM BUFFER



FAN PWM BUFFER_1

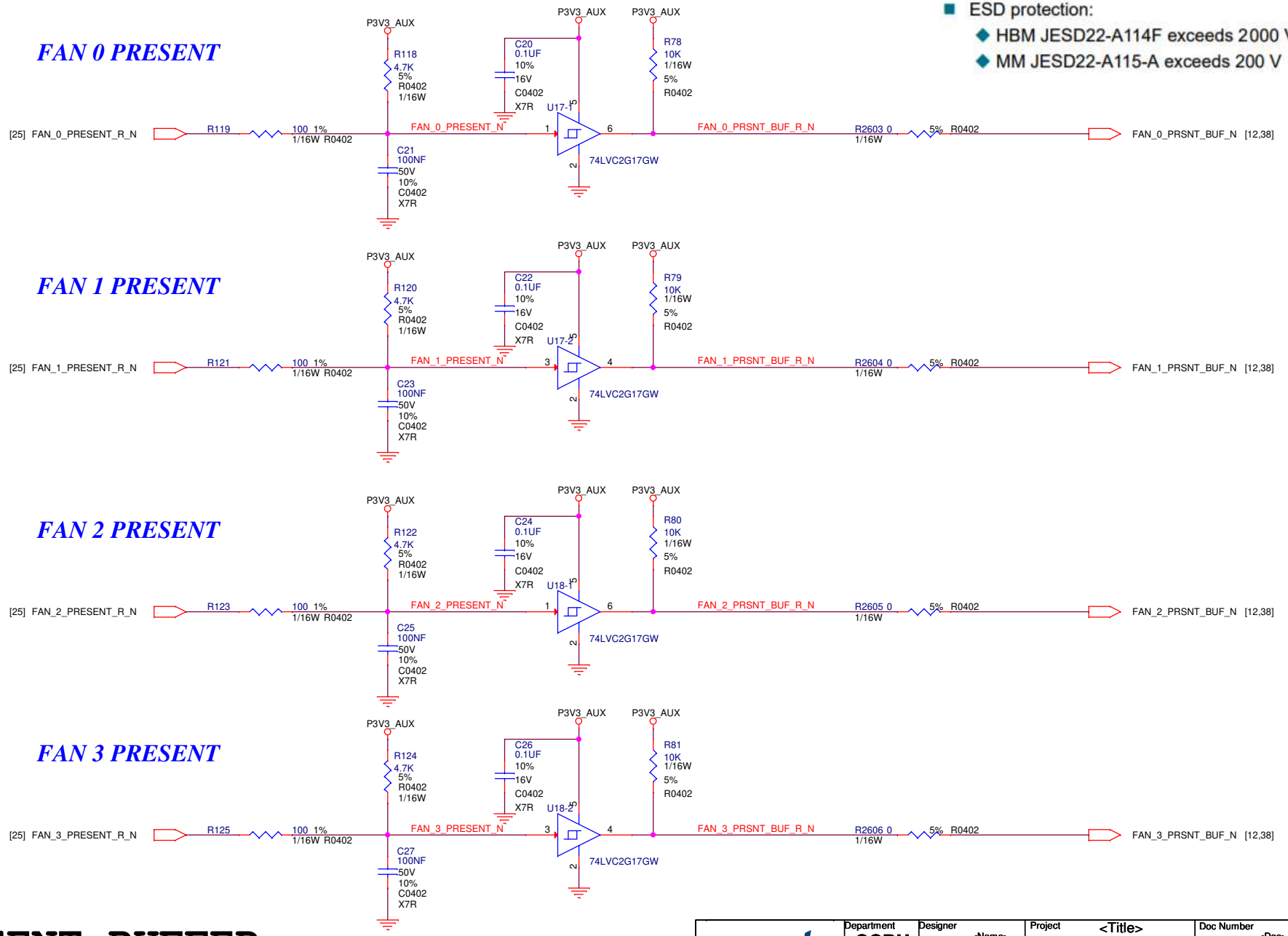
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FAN 2&3 PWM BUFFER



FAN PWM BUFFER_2

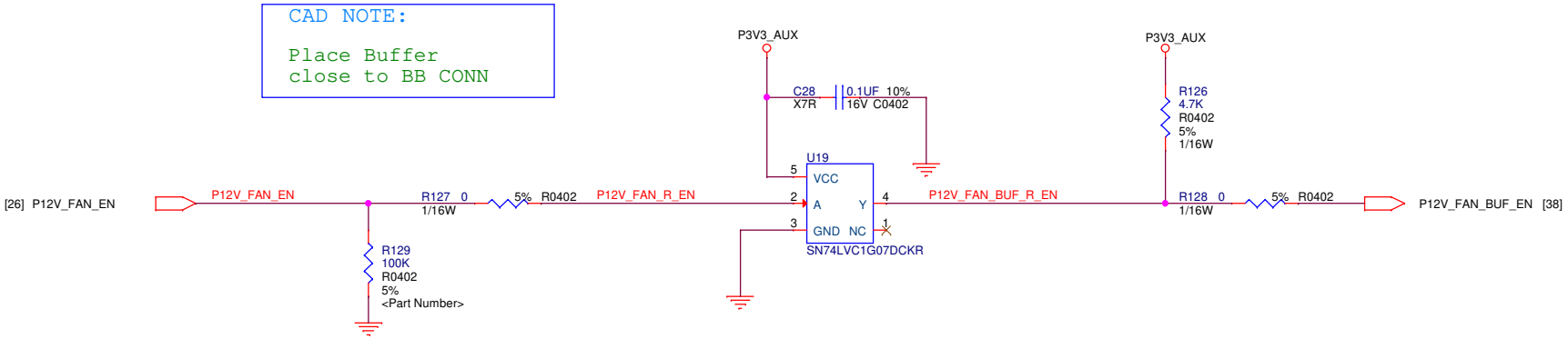
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FAN PRESENT BUFFER

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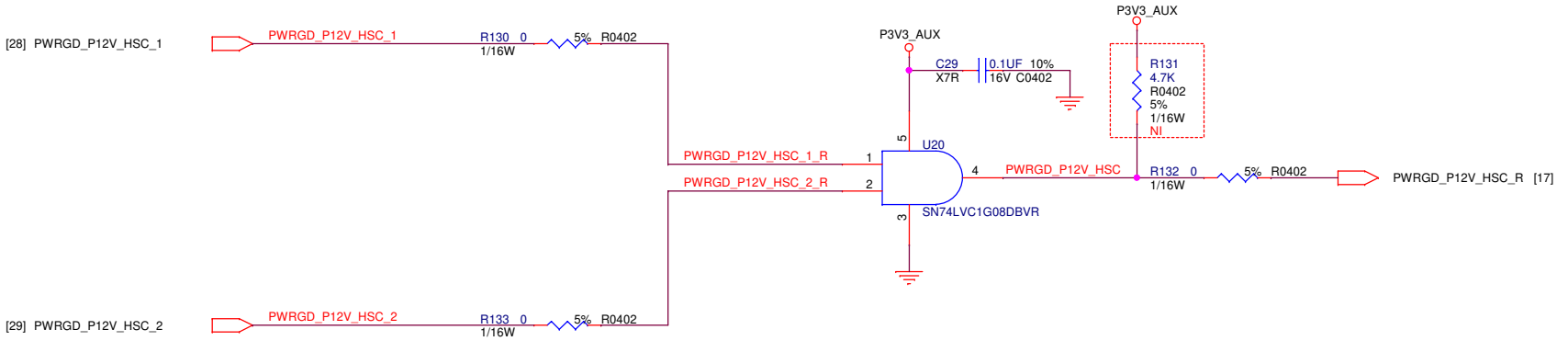
FAN POWER ENABLE



FAN POWER ENABLE BUFFER

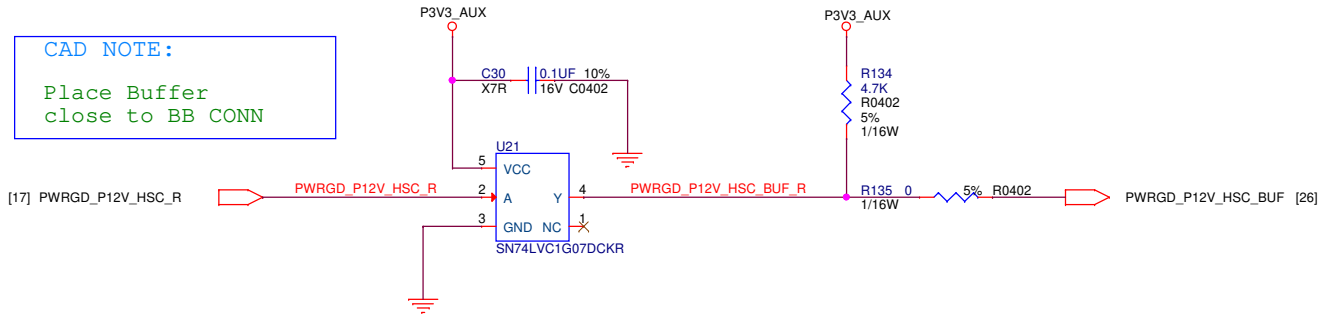
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P12V POWER GOOD BUFFER



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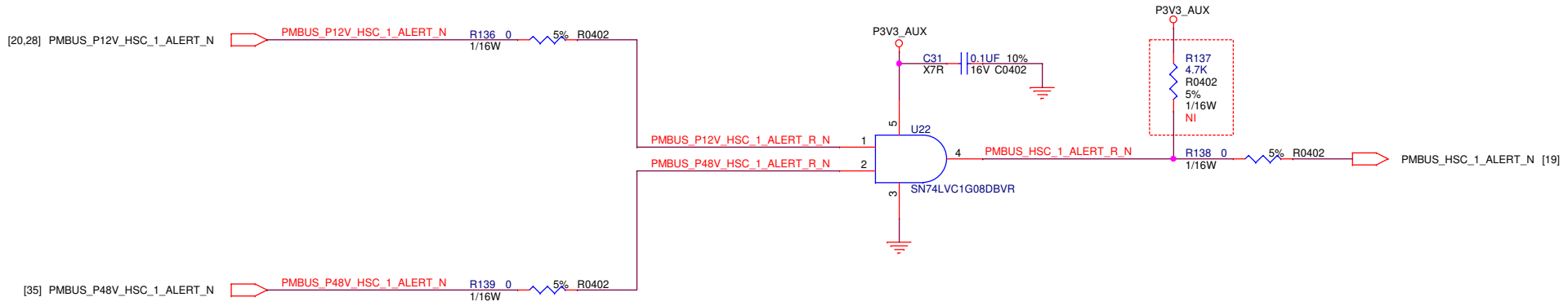
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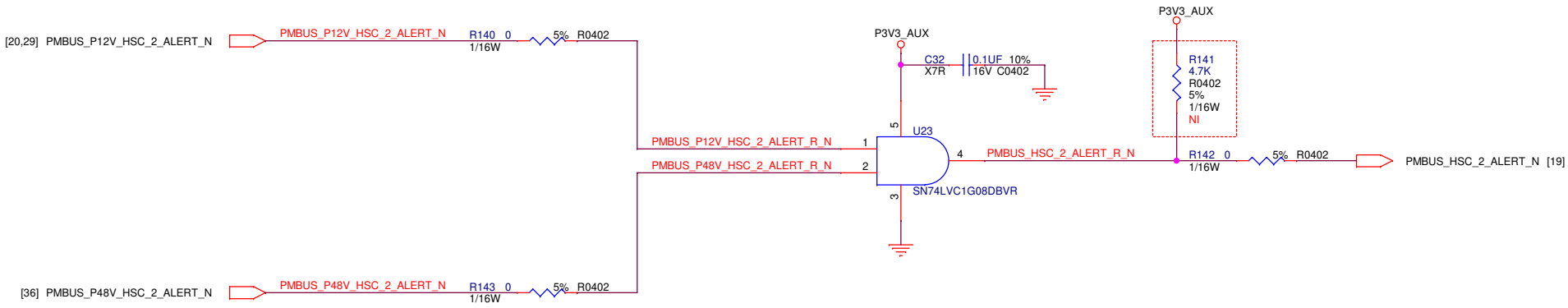
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P12V_1, P48_1 HSC ALERT



P12V_2, P48_2 HSC ALERT



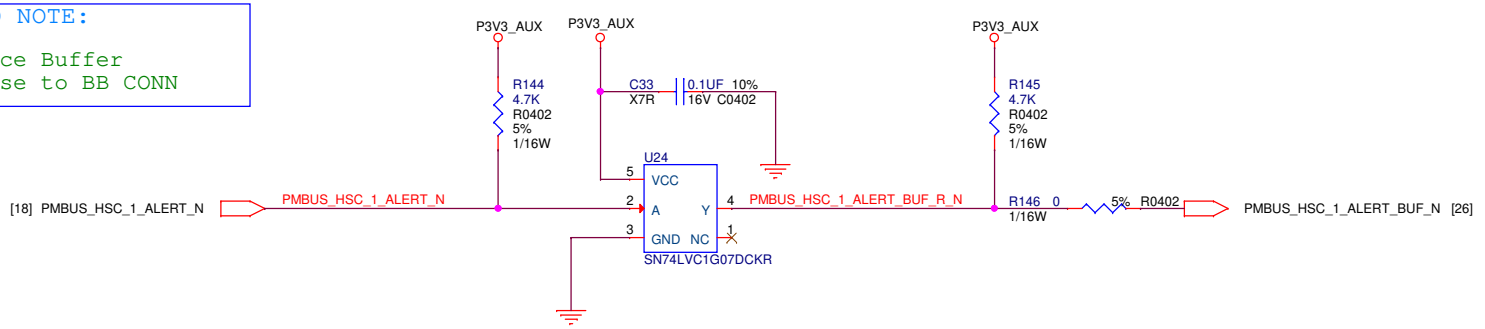
PMBUS HSC ALERT BUFFER_1

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P12V_1, P48_1 HSC ALERT

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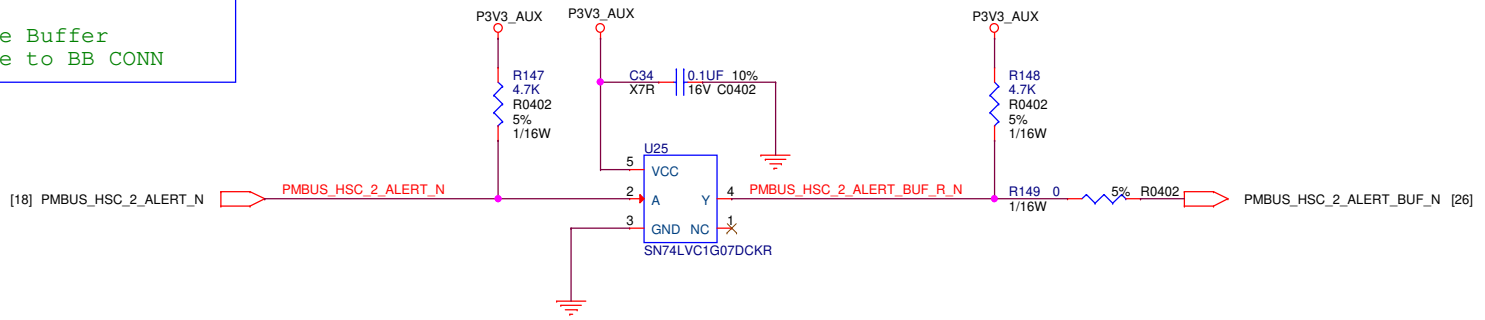
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P12V_2, P48_2 HSC ALERT

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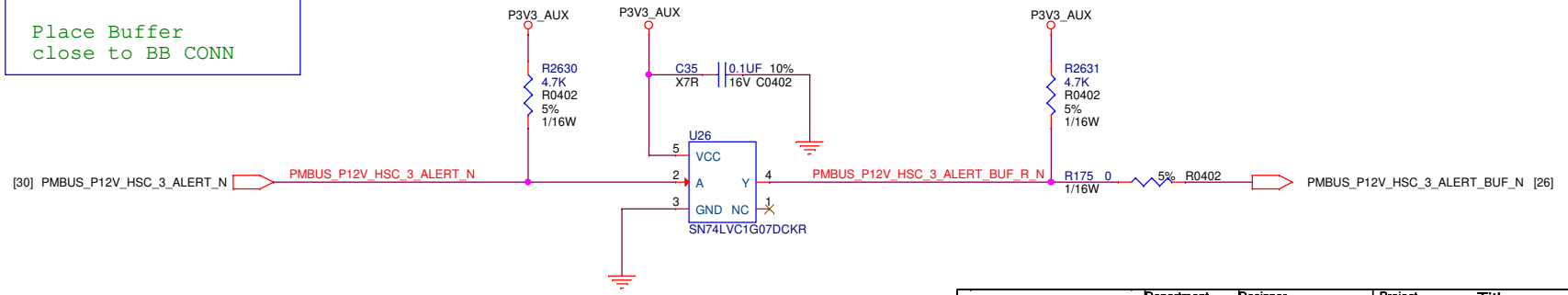
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P12V_AUX HSC ALERT

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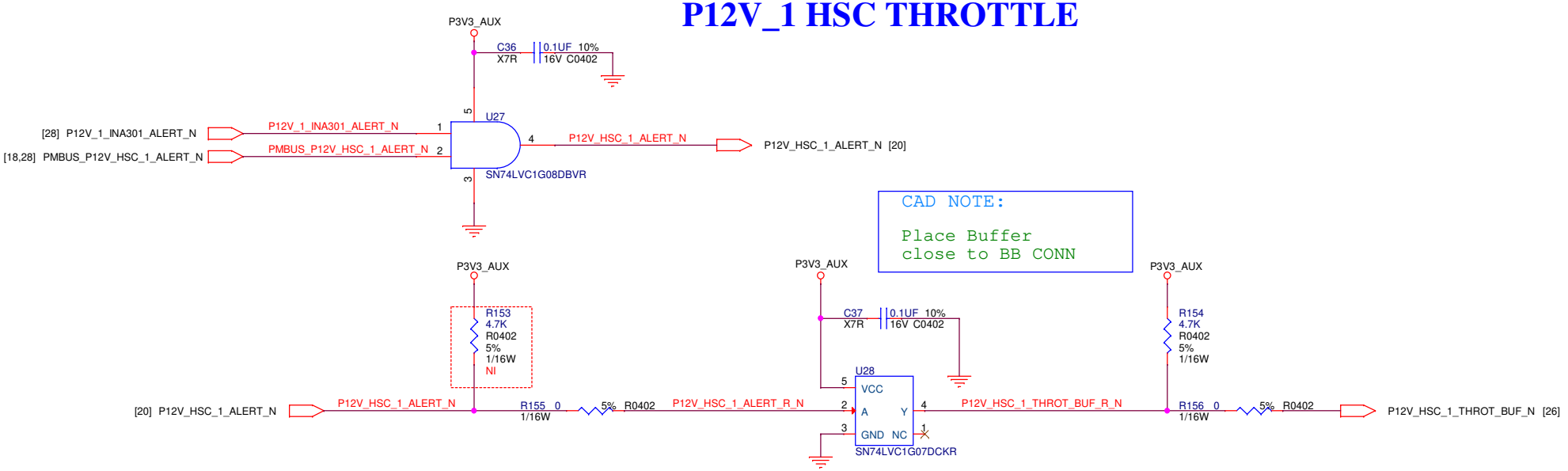
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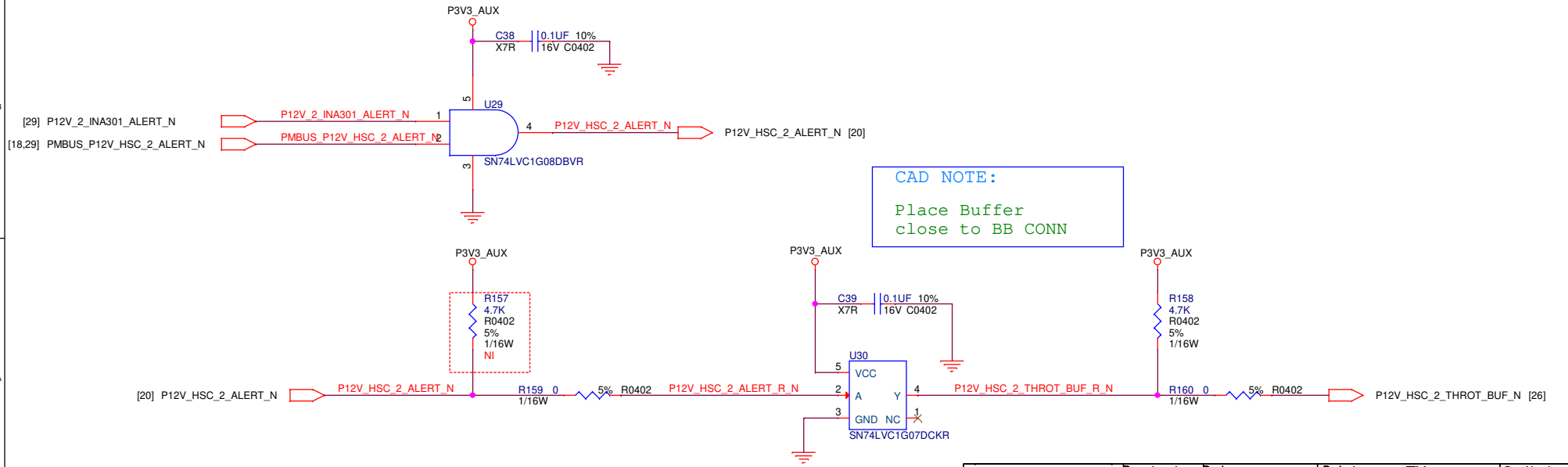
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P12V_1 HSC THROTTLE



P12V_2 HSC THROTTLE



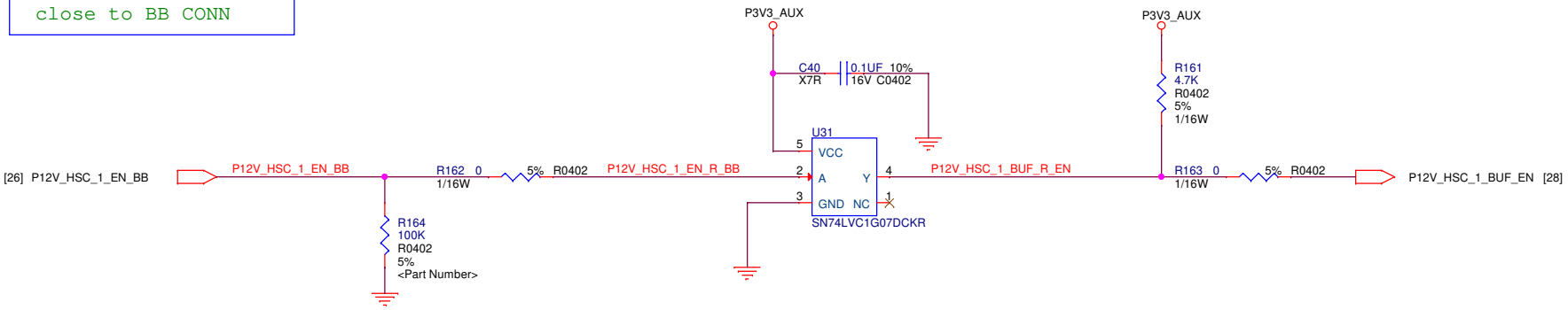
P12V HSC THROTTLE BUFFER

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CAD NOTE:

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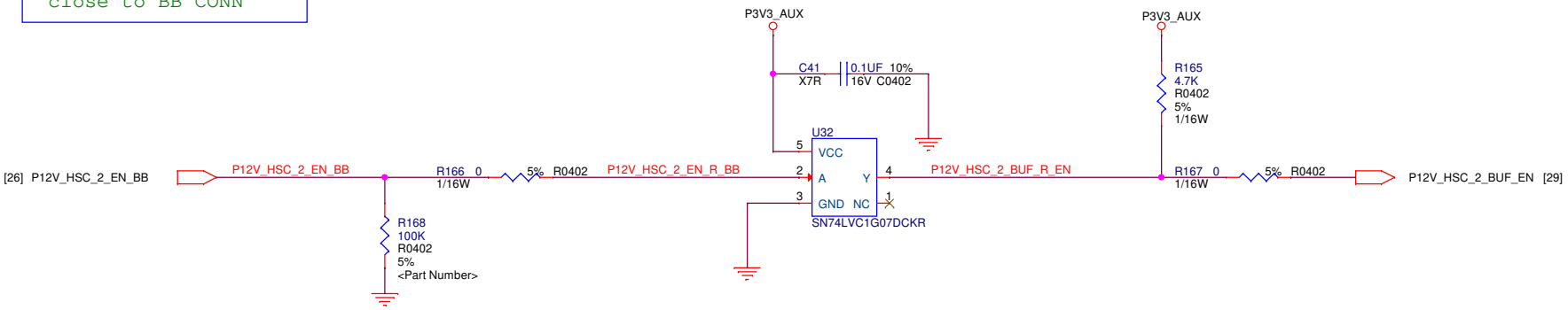
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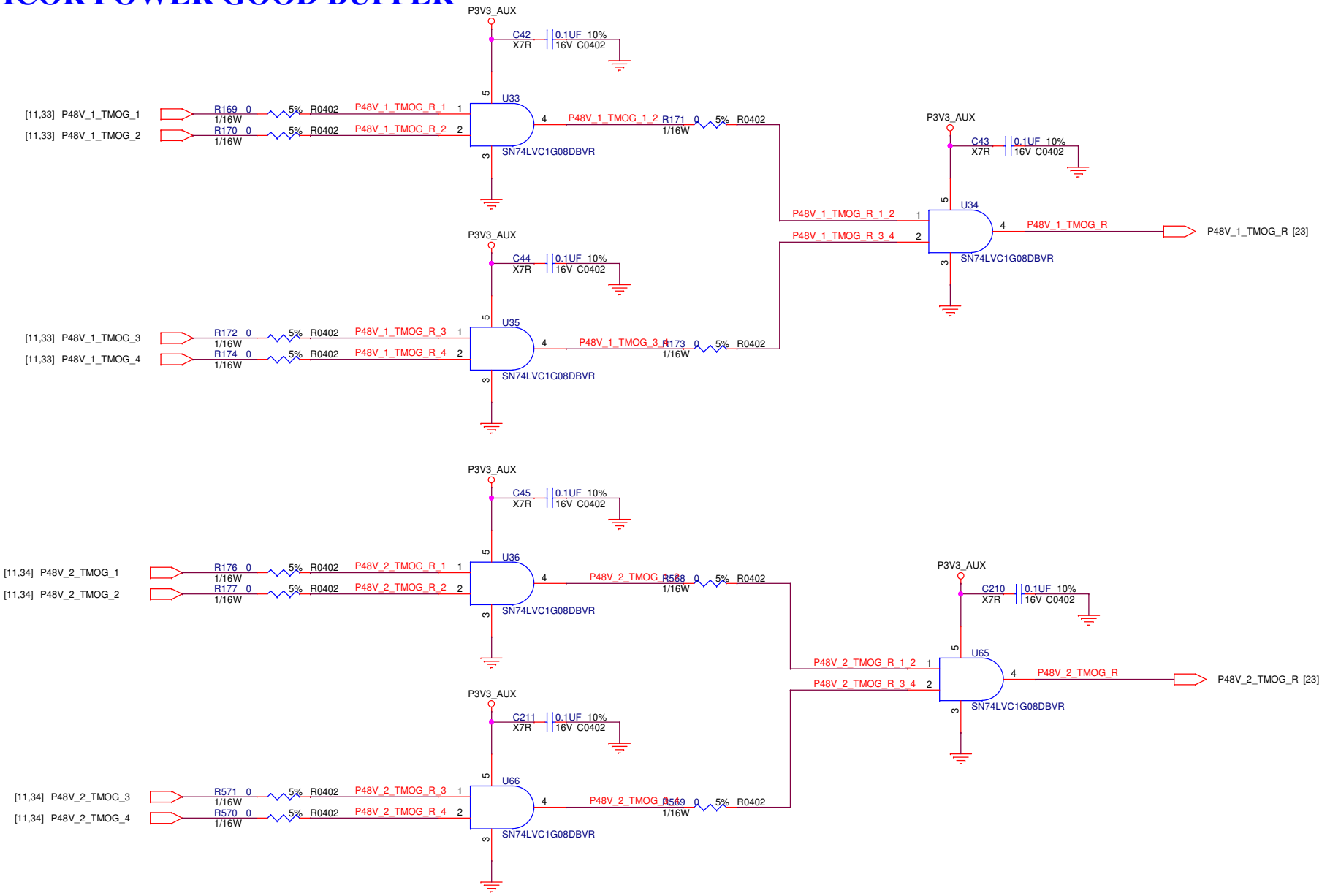
P12V_2 HSC ENABLE



P12V HSC ENABLE BUFFER

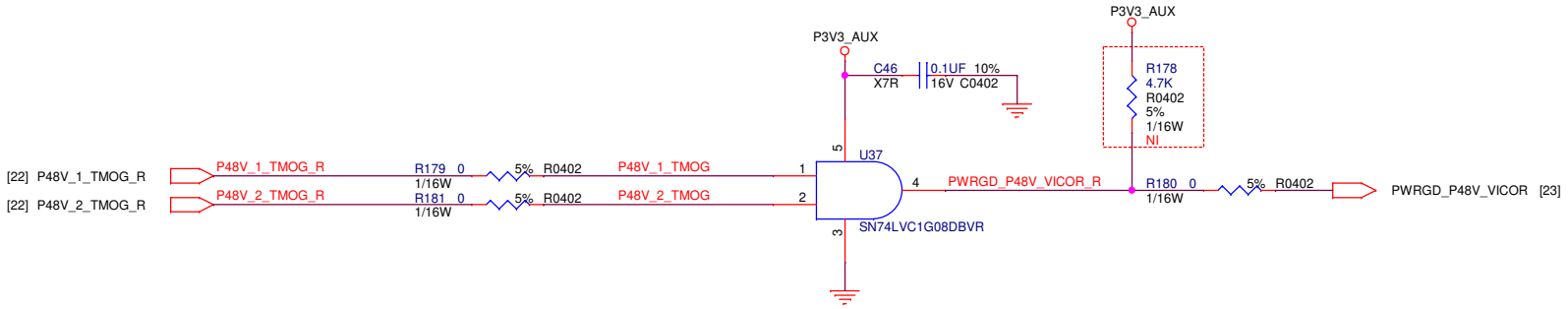
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VICOR POWER GOOD BUFFER



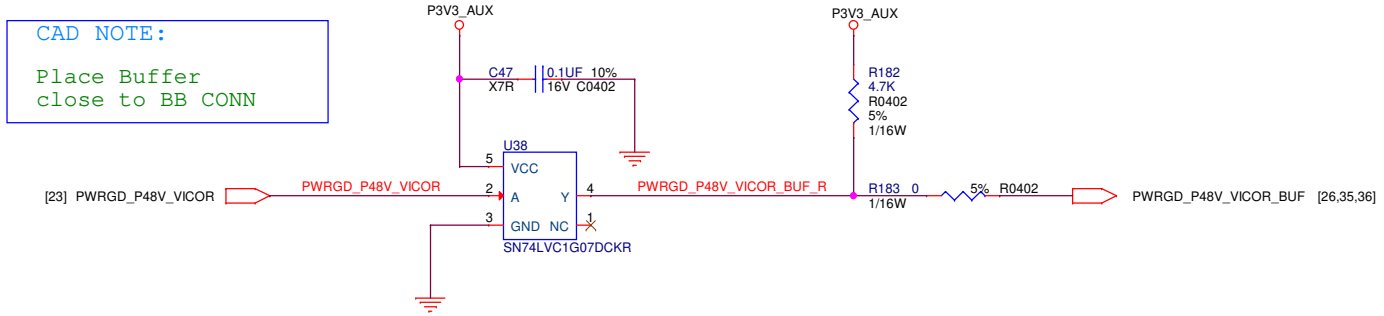
VICOR POWER GOOD BUFFER_1

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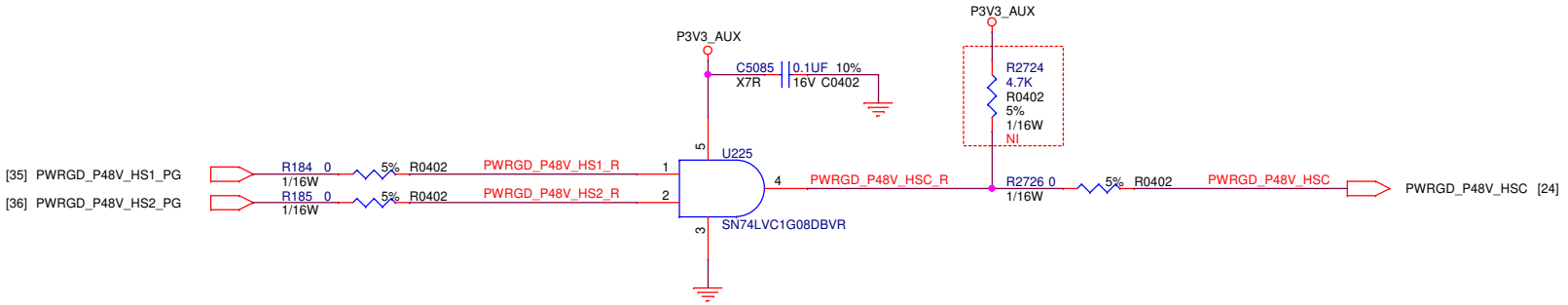
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close to BB CONN



VICOR POWER GOOD BUFFER_2

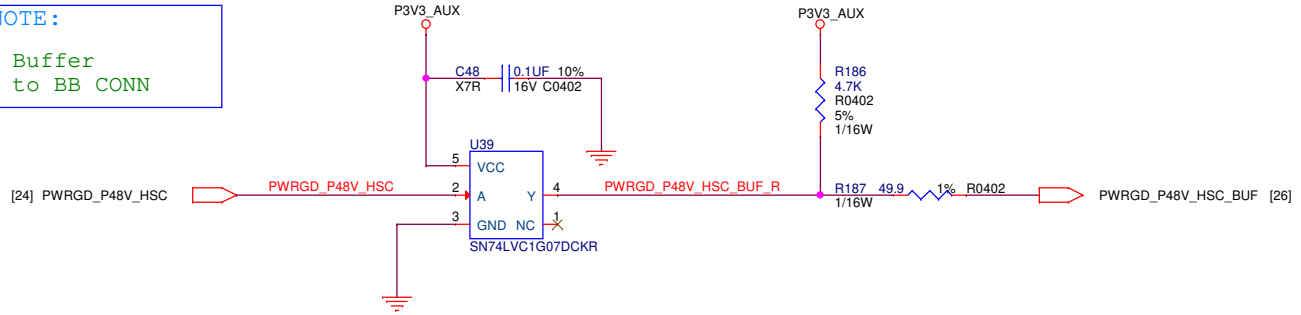
Quanta	Department: CCBU	Designer: <Name>	Project: <Title>	Doc Number: <Doc>	Rev: ?
		Reviewer: <Name>		Page Title: <PageTitle>	
		Size: B	Date: Tuesday, January 18, 2022	Sheet 23 of 43	

P48V POWER GOOD BUFFER



CAD NOTE:

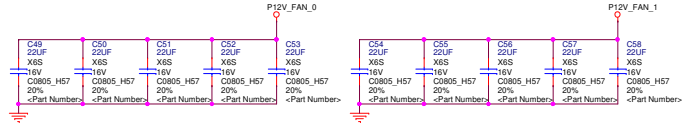
Place Buffer
close to BB CONN

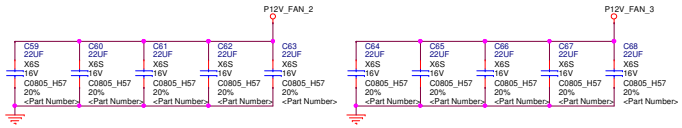


EVT: REMOVE P12V_AUX POWER GOOD BUFFER

P48V POWER GOOD BUFFER

Quanta	Department: CCBU	Designer: <Name>	Project: <Title>	Doc Number: <Doc>	Rev: ?
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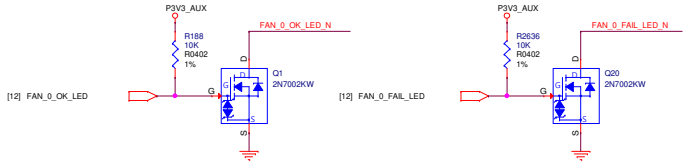


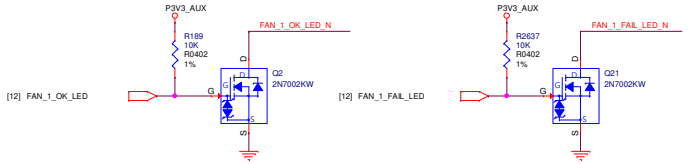
2. ELECTRICAL CHARACTERISTICS

1. CONTACT CURRENT RATING: 1.1AMPS MAX. PER PIN.
2. INSULATION RESISTANCE: 1000 MEGOHMS
3. DIELECTRIC WITHSTANDING VOLTAGE: 500 VAC AT SEA LEVEL.
4. LOW LEVEL CONTACT RESISTANCE (DRY CIRCUIT):
   INITIAL: 30MILLIOHMS MAX.
   AFTER TEST: 50 MILLIOHMS MAX.

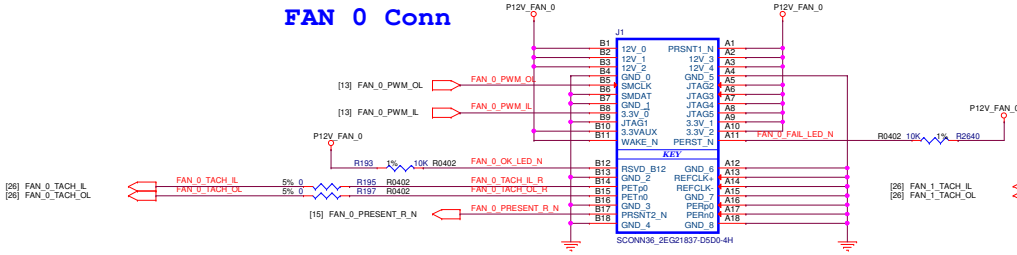
AX5	C
AX6	C

Current Rating: 1.1A/PIN

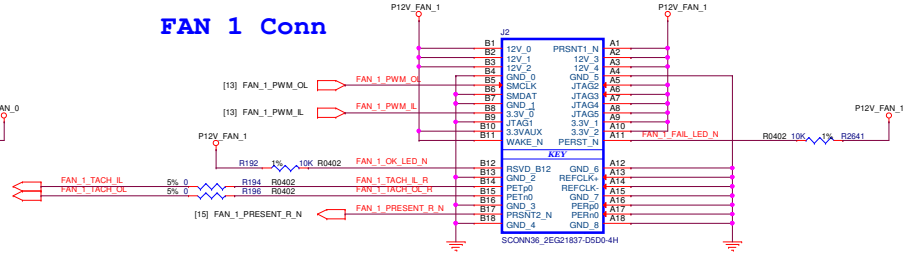


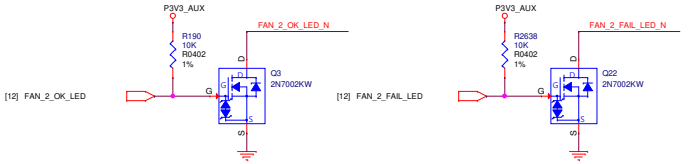


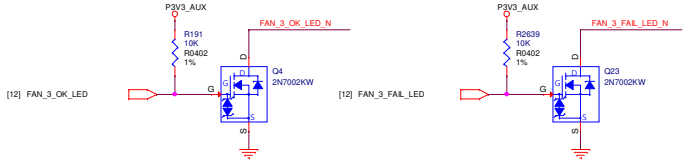
FAN 0 Conn



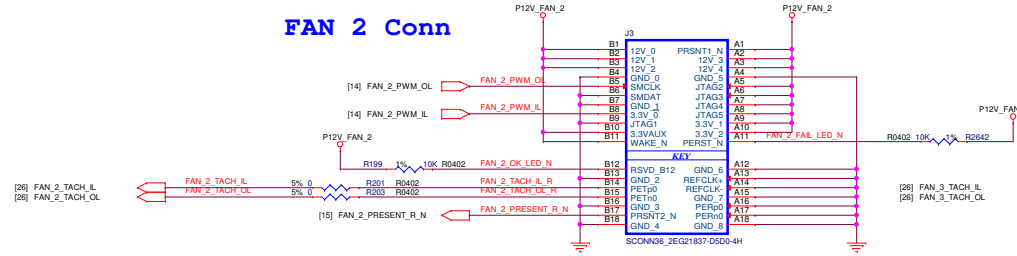
FAN 1 Conn



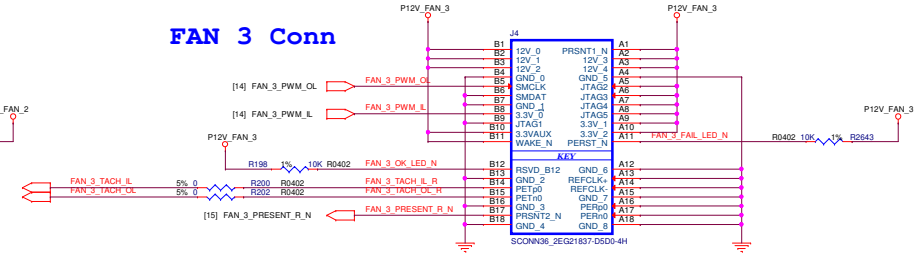




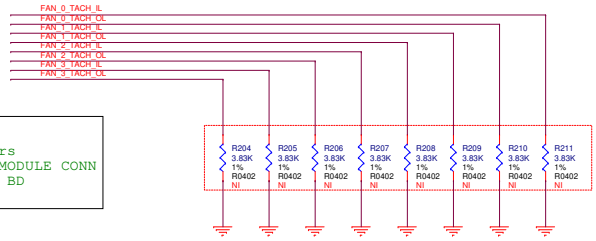
FAN 2 Conn



FAN 3 Conn



FAN TACH



CAD NOTE:

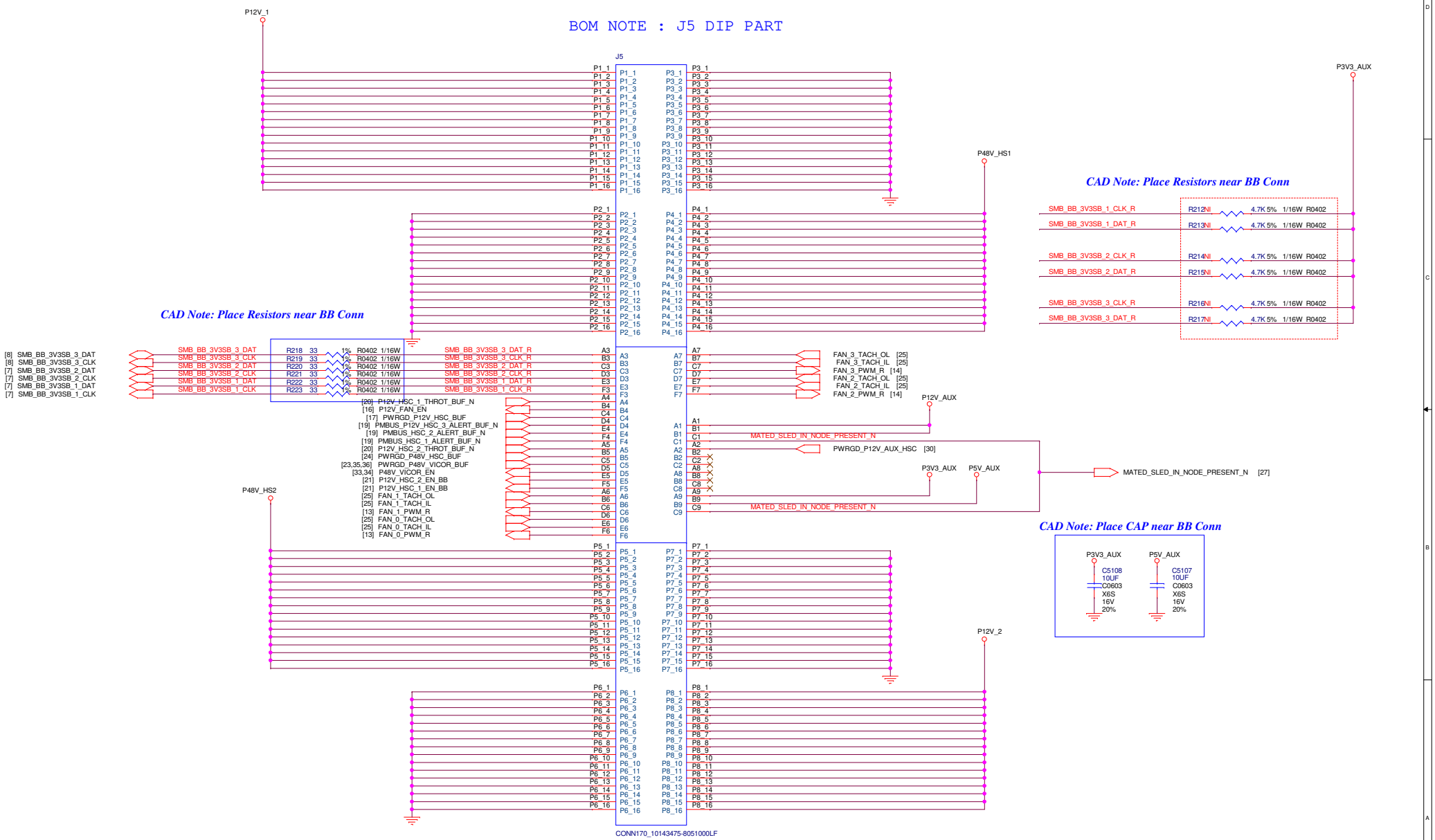
Place resistors
close to FAN MODULE CONN
PU 10K on FAN BD
PD 4.7K on BB

FAN STATUS LED	FAN_0_STATE_LED_N	FAN_0_OK_LED_N	LED on FAN Module
FAN SPEED NORMAL	1	0	GREEN
FAN SPEED ABNORMAL	0	1	RED

TO FAN MODULE CONN

To BB CONN

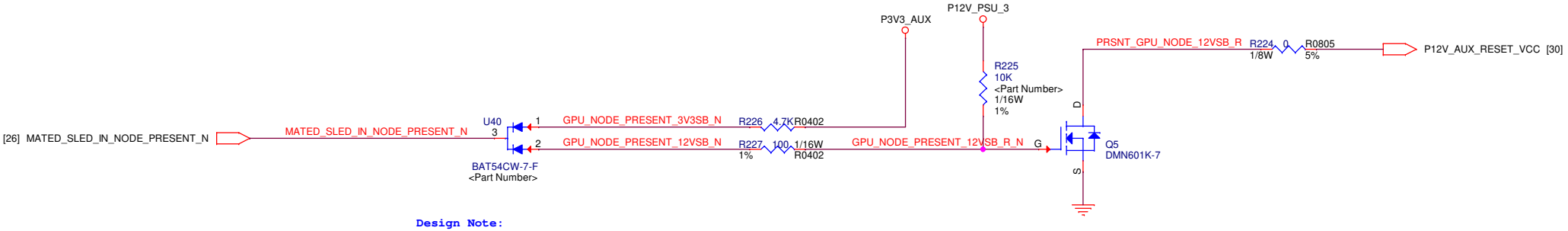
BOM NOTE : J5 DIP PART



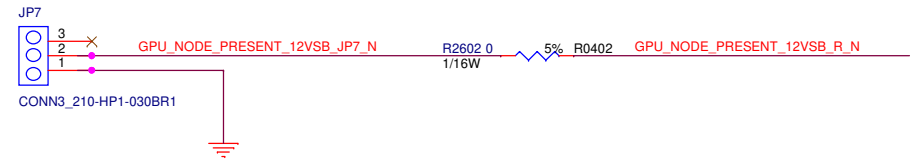
TO BB CONN

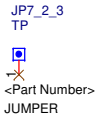
Quanta	Department CCBU	Designer <Name>	Project <Title>	Doc Number <Doc>	Rev ?
		Reviewer <Name>		Page Title	
		Size	Custom Date Tuesday, January 18, 2022	<PageTitle> Sheet 26 of 43	

GPU BB REMOVABLE



Design Note:
1. Only use one present to do GPU BB removable function.
2. When remove GPU BB, all AUX power will be turned off.
3. When insert GPU BB, all AUX power will be turned on.

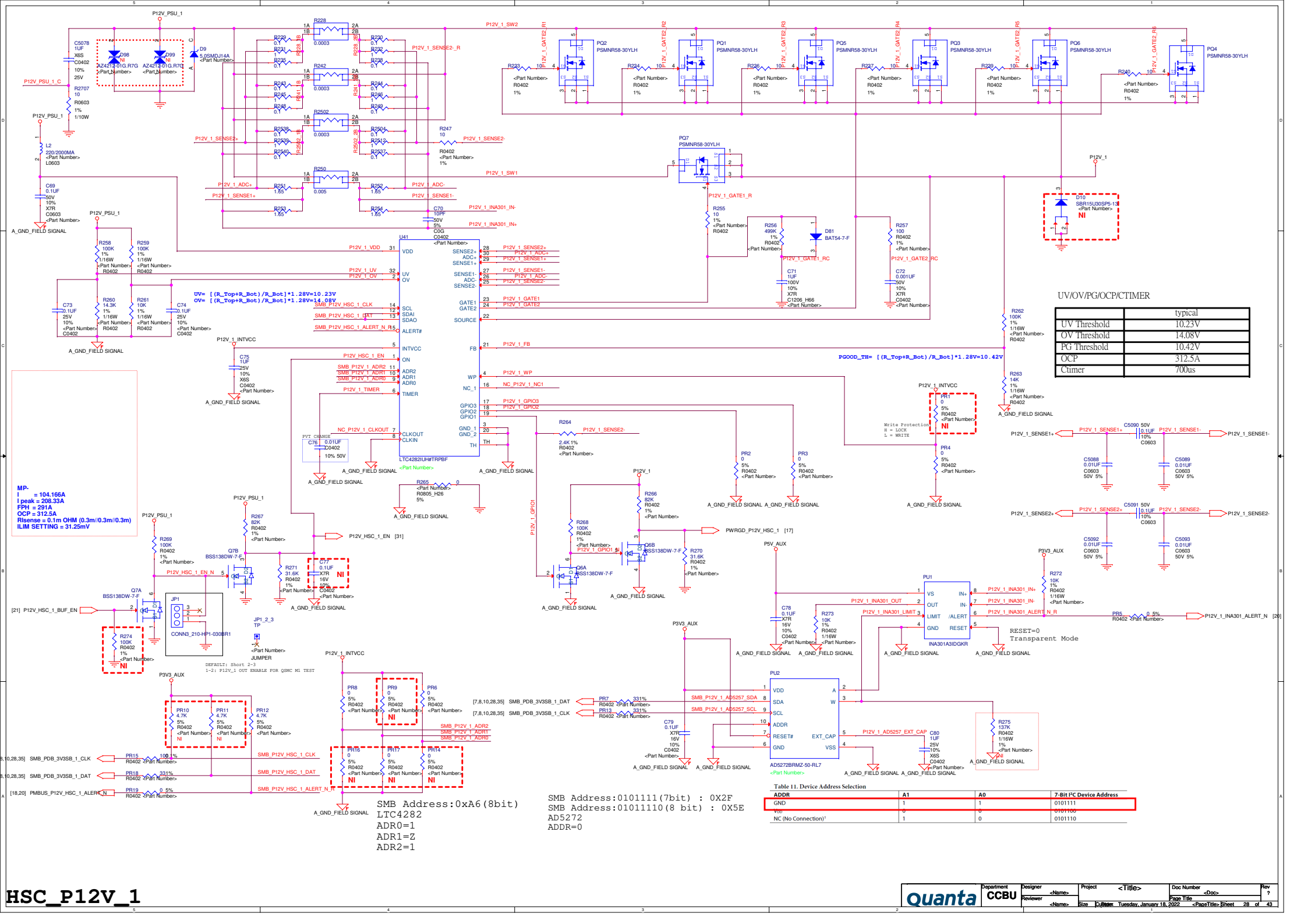


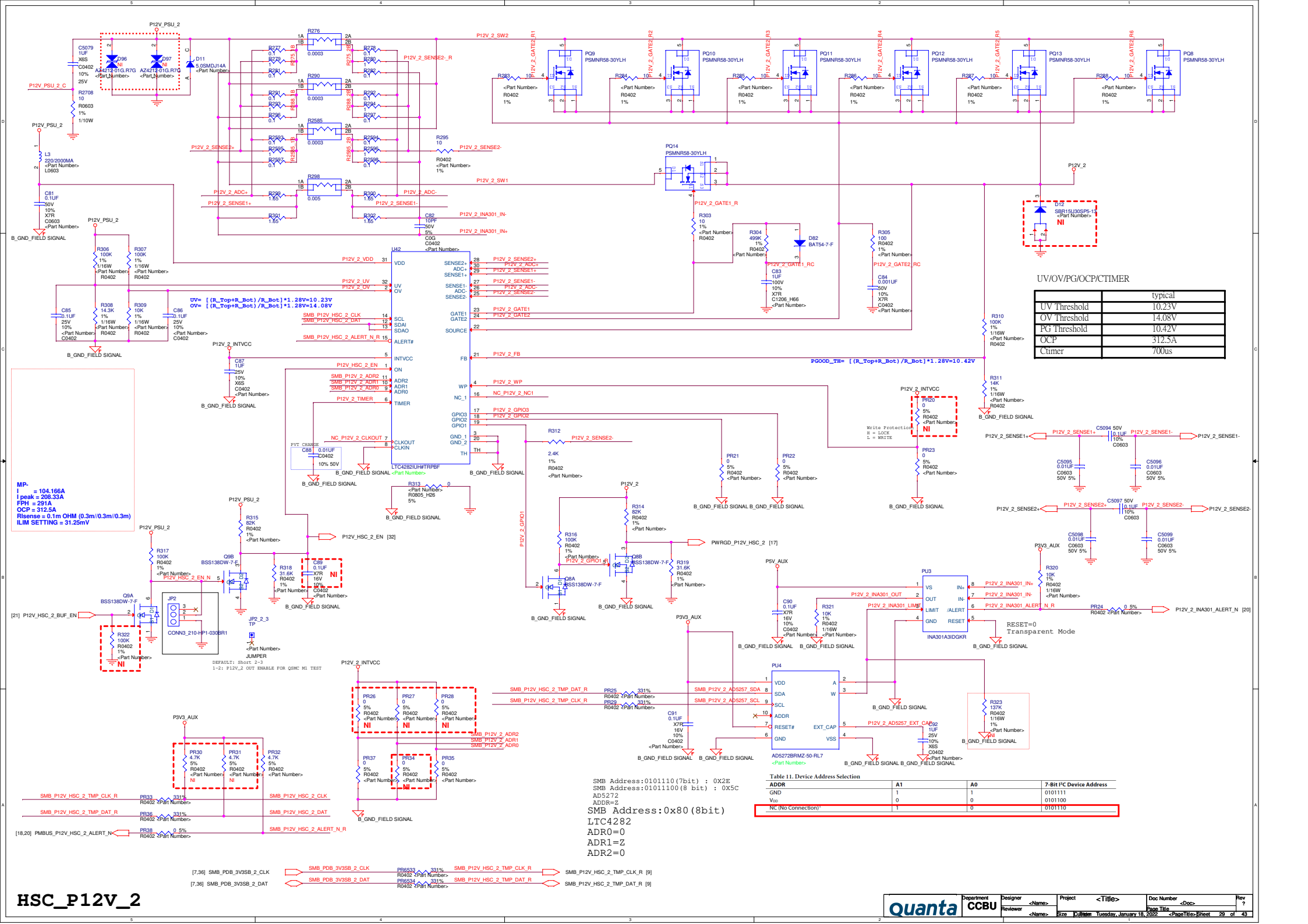


JP7 SELECT
1-2: FORCE ENABLE P12V_AUX
2-3: NORMAL (Default)

GPU BB REMOVABLE

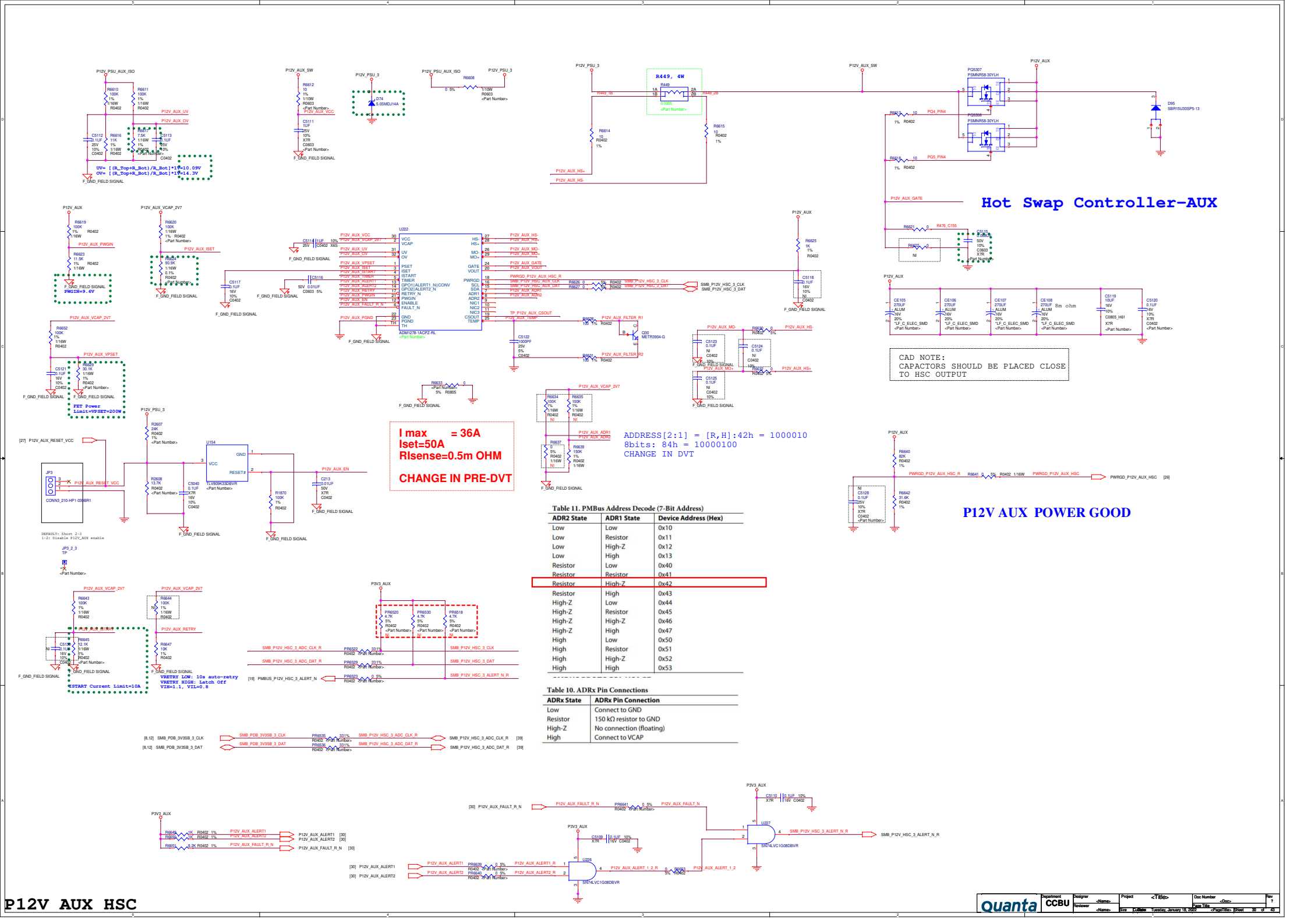
Quanta	Department: CCBU	Designer: <Name>	Project: <Title>	Doc Number: <Doc>	Rev: ?
		Reviewer: <Name>		Page Title: <PageTitle>	
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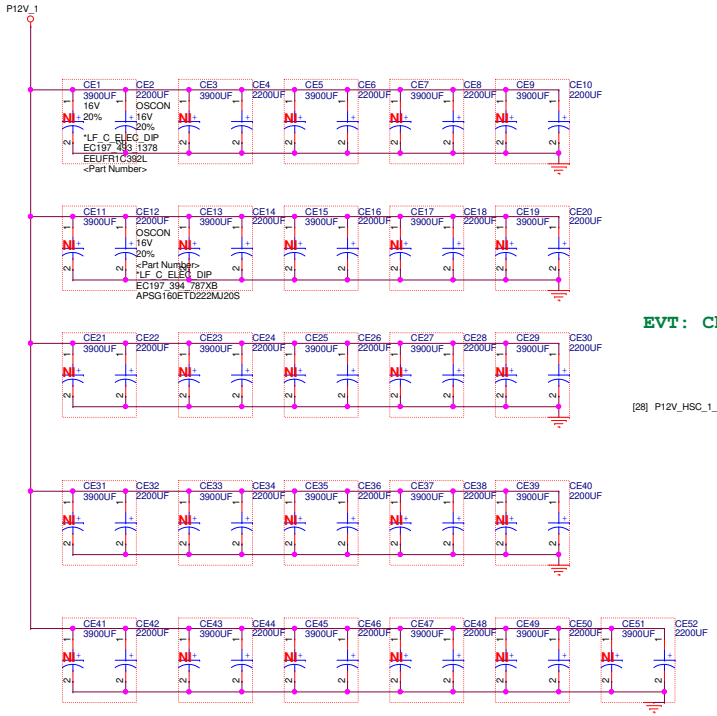

P12V_PSU_1
P12V_PSU_1_C
P12V_PSU_1
L2
220/2000MA
L0603
C69
0.1UF
50V
10%
X7R
C0603
A_GND_FIELD SIGNAL
C5078
1UF
X6S
C0402
10%
25V
R2707
10
R0603
1%
1/10W
D98
NI
AZ4212-01G.R7G
D99
NI
AZ4212-01GLR7G
D9
5.0SMDJ14A
R228
0.0003
R241
0.0003
R242
0.0003
R250
0.005
R247
10
R0402
1%
P12V_1_SENSE2-_R
P12V_1_SENSE2-
P12V_1_SENSE2+
P12V_1_ADC+
P12V_1_SENSE1+
P12V_1_ADC-
P12V_1_SENSE1-
P12V_1_SW1
P12V_1_SW2
P12V_1_GATE1_R1
P12V_1_GATE1_R2
P12V_1_GATE1_R3
P12V_1_GATE1_R4
P12V_1_GATE2_R5
P12V_1_GATE2_R6
PQ2
PSMNR58-30YLH
PQ1
PSMNR58-30YLH
PQ5
PSMNR58-30YLH
PQ3
PSMNR58-30YLH
PQ6
PSMNR58-30YLH
PQ4
PSMNR58-30YLH
PQ7
PSMNR58-30YLH
P12V_1_GATE1_R
P12V_1_GATE1_RC
P12V_1_GATE2_RC
R255
10
R256
499K
D81
BAT54-7-F
R257
100
C71
1UF
100V
C1206_H66
C72
0.001UF
50V
C0402
P12V_1
D10
SBR15U30SPS-13
NI
U41
LTC4282IUH#TRPBF
P12V_1_VDD
P12V_1_UV
P12V_1_OV
SMB_P12V_HSC_1_CLK
SMB_P12V_HSC_1_DAT
SMB_P12V_HSC_1_ALERT_N_R
P12V_1_INTVCC
P12V_HSC_1_EN
SMB_P12V_1_ADR2
SMB_P12V_1_ADR1
SMB_P12V_1_ADR0
P12V_1_TIMER
NC_P12V_1_CLKOUT
P12V_1_GATE1
P12V_1_GATE2
P12V_1_FB
P12V_1_WP
NC_P12V_1_NC1
P12V_1_GPIO3
P12V_1_GPIO2
P12V_1_SENSE2-
UV= [(R_Top+R_Bot)/R_Bot]*1.28V=10.23V
OV= [(R_Top+R_Bot)/R_Bot]*1.28V=14.08V
PGOOD_TH= [(R_Top+R_Bot)/R_Bot]*1.28V=10.42V
UV/OV/PG/OCP/CTIMER
typical
UV Threshold 10.23V
OV Threshold 14.08V
PG Threshold 10.42V
OCP 312.5A
Ctimer 700us
MP-
I = 104.166A
I peak = 208.33A
FPH = 291A
OCP = 312.5A
Risense = 0.1m OHM (0.3m//0.3m//0.3m)
ILIM SETTING = 31.25mV
P12V_HSC_1_EN [31]
PWRGD_P12V_HSC_1 [17]
P5V_AUX
P3V3_AUX
PU1
INA301A3IDGKR
P12V_1_INA301_IN+
P12V_1_INA301_IN-
P12V_1_INA301_OUT
P12V_1_INA301_LIMIT
P12V_1_INA301_ALERT_N_R
P12V_1_INA301_ALERT_N [20]
RESET=0
Transparent Mode
JP1
CONN3_210-HP1-0308R1
JP1_2_3
TP
JUMPER
DEFAULT: Short 2-3
1-2: P12V_1 OUT ENABLE FOR QSMC M1 TEST
[21] P12V_HSC_1_BUF_EN
PU2
AD5272BRMZ-50-RL7
SMB_P12V_1_AD5257_SDA
SMB_P12V_1_AD5257_SCL
P12V_1_AD5257_EXT_CAP
[7,8,10,28,35] SMB_PDB_3V3SB_1_DAT
[7,8,10,28,35] SMB_PDB_3V3SB_1_CLK
[18,20] PMBUS_P12V_HSC_1_ALERT_N
SMB_P12V_HSC_1_CLK
SMB_P12V_HSC_1_DAT
SMB_P12V_HSC_1_ALERT_N
SMB Address:0xA6(8bit)
LTC4282
ADR0=1
ADR1=Z
ADR2=1
SMB Address:0101111(7bit) : 0X2F
SMB Address:01011110(8 bit) : 0X5E
AD5272
ADDR=0
Table 11. Device Address Selection
ADDR | A1 | A0 | 7-Bit I²C Device Address
GND | 1 | 1 | 0101111
VDD | 0 | 0 | 0101100
NC (No Connection)[1] | 1 | 0 | 0101110
HSC_P12V_1
Quanta
CCBU
Tuesday, January 18, 2022
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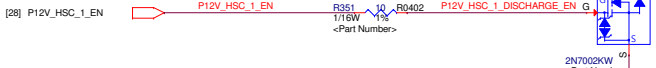
HSC_P12V_2

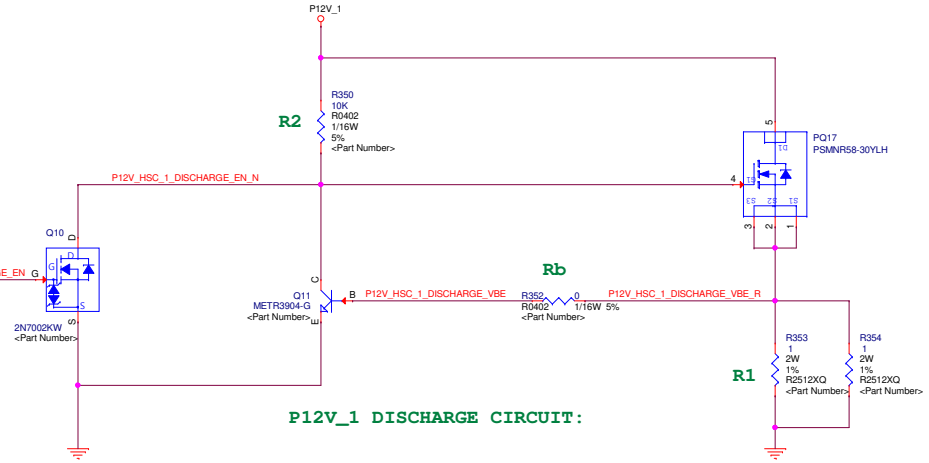
Quanta	Department CCBU	Designer <Name>	Project <Title>
		Reviewer <Name>	Doc Number <Doc> Rev ?
			Page Title
		Size C Date: Tuesday, January 18, 2022	<PageTitle> Sheet 29 of 43


Hot Swap Controller-AUX
CAD NOTE:
CAPACTORS SHOULD BE PLACED CLOSE
TO HSC OUTPUT
I max = 36A
Iset=50A
RIsense=0.5m OHM
CHANGE IN PRE-DVT
ADDRESS[2:1] = [R,H]:42h = 1000010
8bits: 84h = 10000100
CHANGE IN DVT
P12V AUX POWER GOOD
P12V AUX HSC
Table 11. PMBus Address Decode (7-Bit Address)
ADR2 State | ADR1 State | Device Address (Hex)
Low | Low | 0x10
Low | Resistor | 0x11
Low | High-Z | 0x12
Low | High | 0x13
Resistor | Low | 0x40
Resistor | Resistor | 0x41
Resistor | High-Z | 0x42
Resistor | High | 0x43
High-Z | Low | 0x44
High-Z | Resistor | 0x45
High-Z | High-Z | 0x46
High-Z | High | 0x47
High | Low | 0x50
High | Resistor | 0x51
High | High-Z | 0x52
High | High | 0x53
Table 10. ADRx Pin Connections
ADRx State | ADRx Pin Connection
Low | Connect to GND
Resistor | 150 kΩ resistor to GND
High-Z | No connection (floating)
High | Connect to VCAP
Quanta
CCBU



EVT: Change to P12V_HSC_1_EN



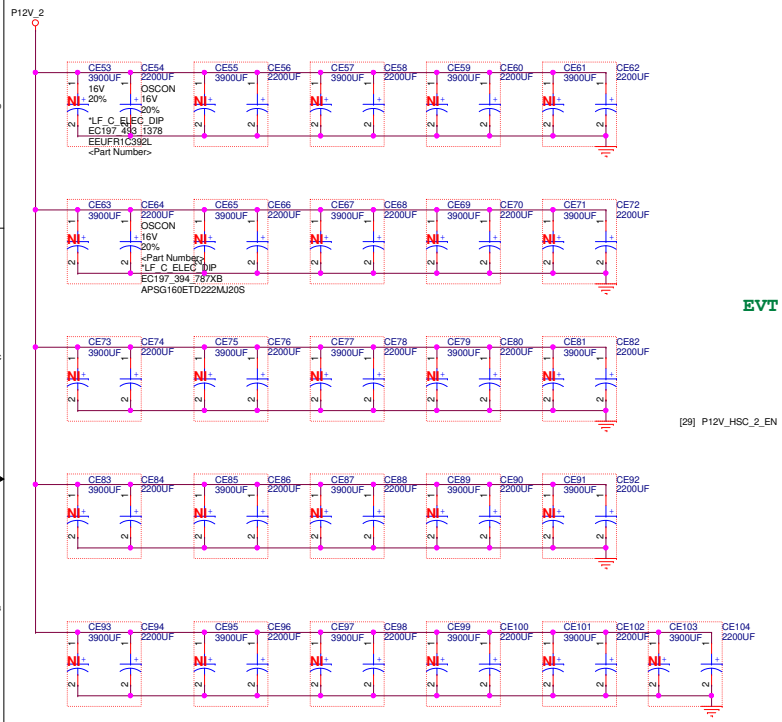


P12V_1 DISCHARGE CIRCUIT:

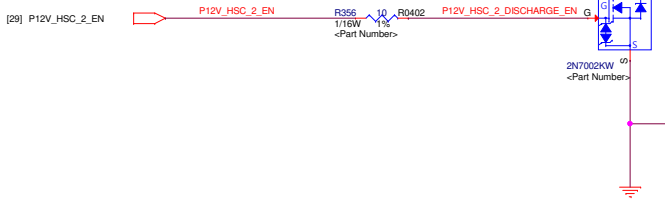
CAD NOTE:
1. CAPACTORS SHOULD BE PLACED CLOSE TO HSC OUTPUT
2. These caps are for pre-layout size, real spec is 3900UF@12mohm ESR.
3. Red rectangle means need to do co-lay.

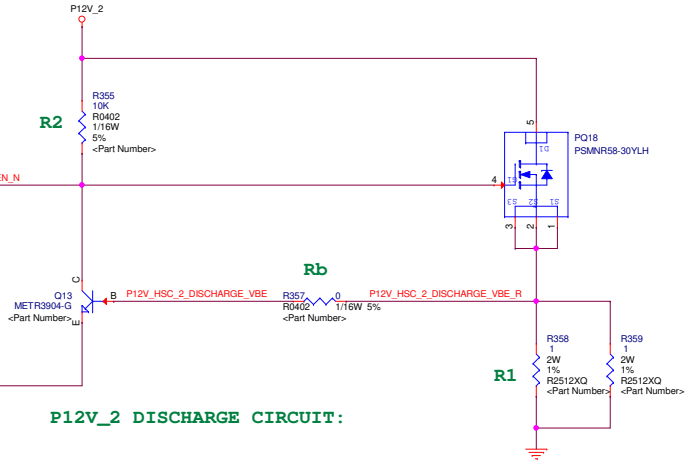
ECAP_P12V_1

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		Reviewer: <Name>		Page Title: <PageTitle>	
			Size: Custom	Date: Tuesday, January 18, 2022	Sheet 31 of 43



EVT: Change to P12V_HSC_2_EN





P12V_2 DISCHARGE CIRCUIT:

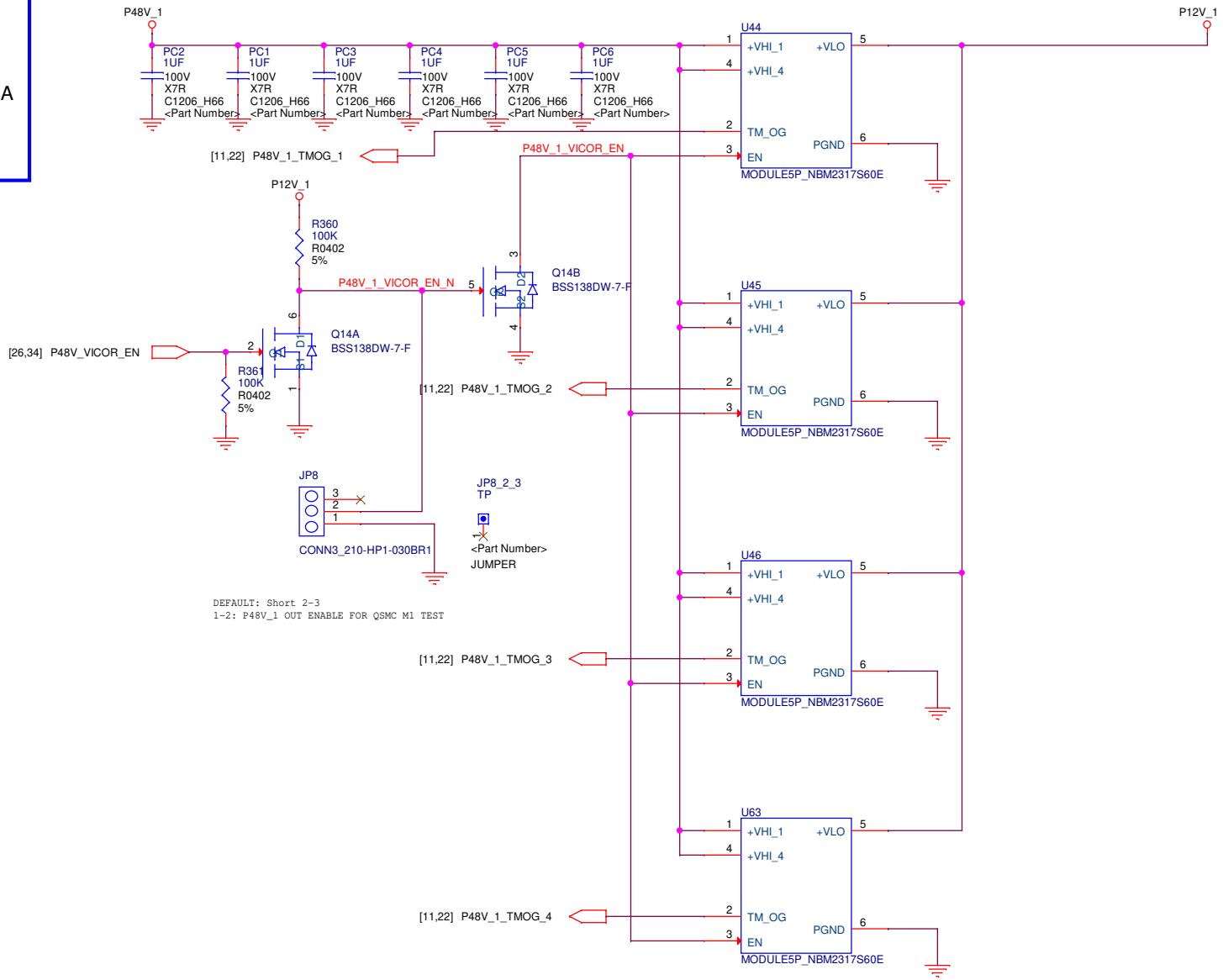
CAD NOTE:
1. CAPACTORS SHOULD BE PLACED CLOSE TO HSC OUTPUT
2. These caps are for pre-layout size, real spec is 3900UF@12mohm ESR.
3. Red rectangle means need to do co-lay.

ECAP_P12V_2

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		Reviewer: <Name>		Page Title: <PageTitle>	
			Size	Date: Tuesday, January 18, 2022	Sheet 32 of 43

Design specification

Output Voltage = 48V±5%
Output Ripple & Noise < 480mV
Transient Tolerance = 4.8V
TDC = 25A
Max current = 31A
Over-Current Protection(IC rating) = 75A
Current Step = 16A
Slew Rate = 10A/us
Efficiency > 96.5% @TDC

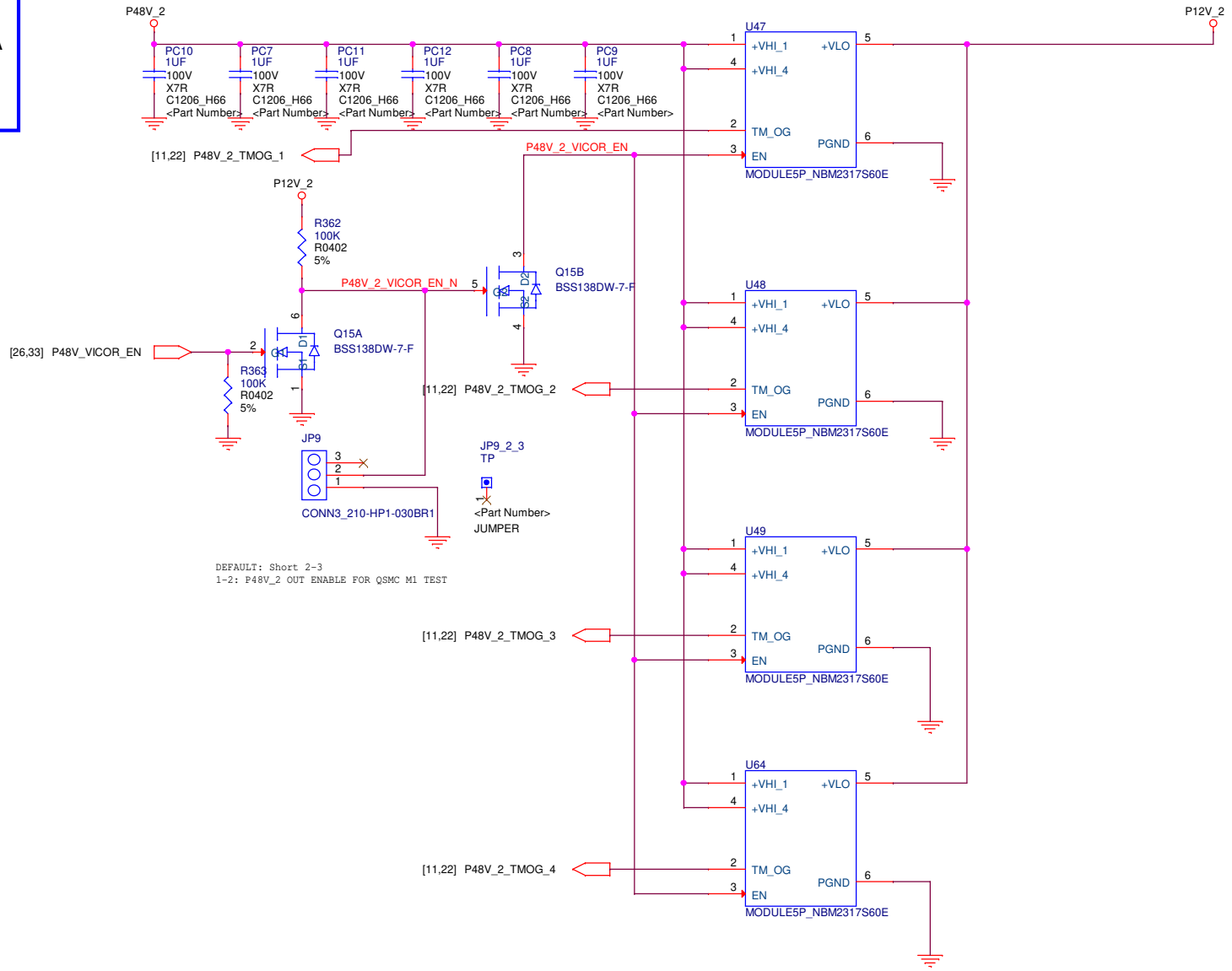


P48V_1

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		Reviewer: <Name>		Page Title: <PageTitle>
		Size: B Date: Tuesday, January 18, 2022		Sheet 33 of 43

Design specification

Output Voltage = 48V±5%
Output Ripple & Noise < 480mV
Transient Tolerance = 4.8V
TDC = 25A
Max current = 31A
Over-Current Protection(IC rating) = 75A
Current Step = 16A
Slew Rate = 10A/us
Efficiency > 96.5% @TDC



P48V_2

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		Reviewer: <Name>		Page Title:
		Size: B Date: Tuesday, January 18, 2022	<PageTitle>	Sheet 34 of 43

48V_1 HOT SWAP_ADM1272

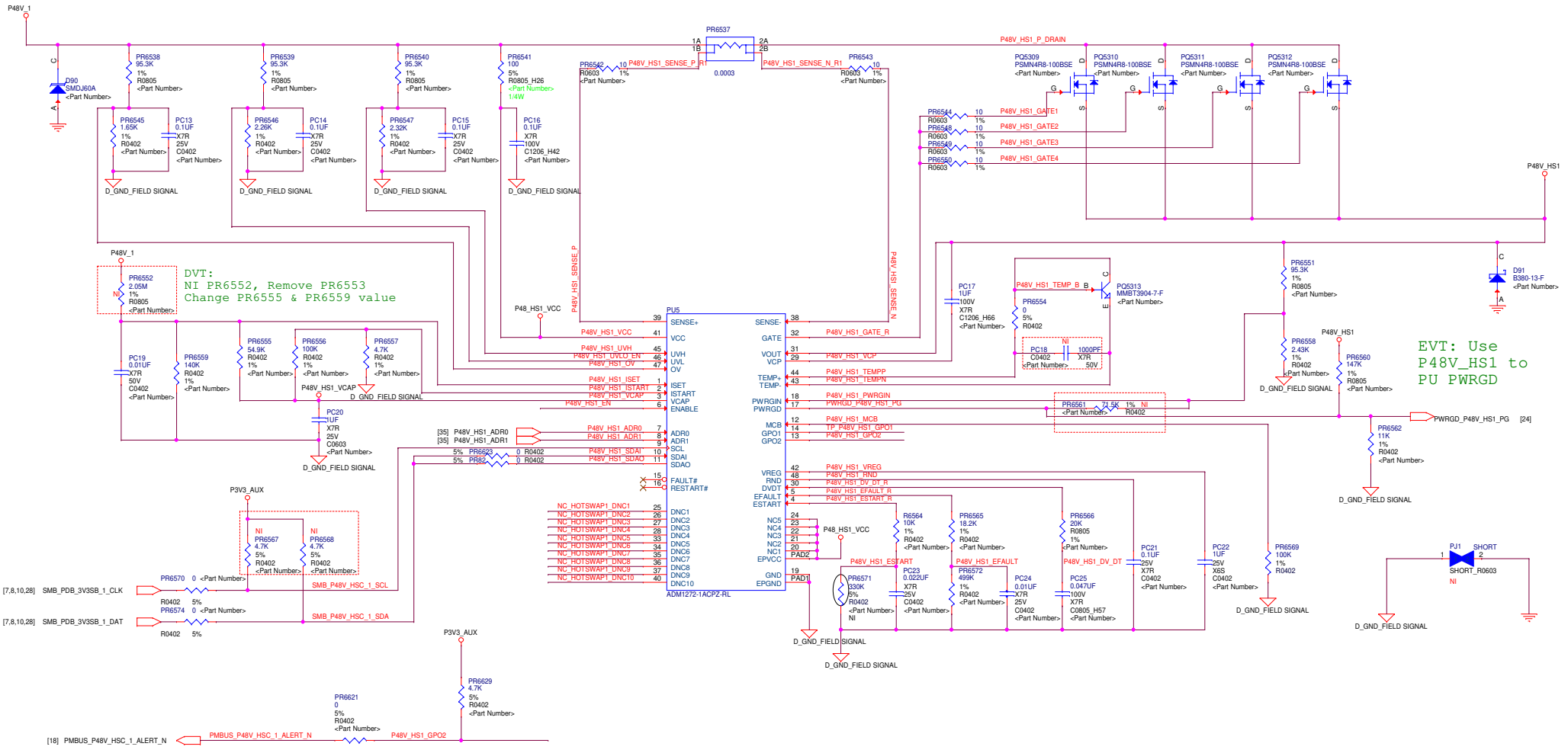
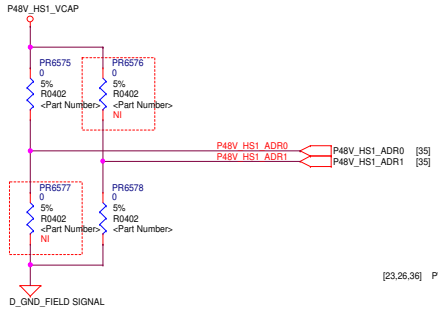


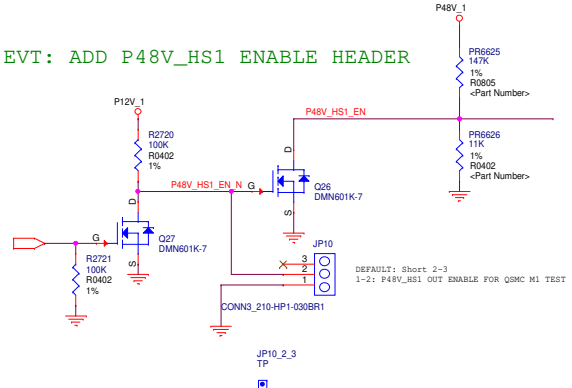
Table 9. PMBus Address Decode (7-Bit Address)

ADR2 State	ADR1 State	Device Address
Low	Low	0x10
Low	Resistor	0x11
Low	High-Z	0x12
Low	High	0x13
Resistor	Low	0x14
Resistor	Resistor	0x15
Resistor	High-Z	0x16
Resistor	High	0x17
High-Z	Low	0x18
High-Z	Resistor	0x19
High-Z	High-Z	0x1A
High-Z	High	0x1B
High	Low	0x1C
High	Resistor	0x1D
High	High-Z	0x1E
High	High	0x1F



SMB Address:0x13(7bit),0x26(8bit)
ADR0=1
ADR1=0

EVT: ADD P48V_HS1 ENABLE HEADER



UV/OV/PG Thresholds

	min.	typical	max.
Rising UVLO	41.893	43.168	44.443
Falling UVLO	38.360	39.710	41.060
Rising OVLO	58.052	59.827	61.602
Falling OVLO	57.51	59.35	61.19
Rising PG	NA	42.12	NA
Falling PG	NA	39.74	NA

Unit: V

Current Limit & Circuit breaker

Resulting Current Limit: 3KW (63A)

48V_2 HOT SWAP_ADM1272

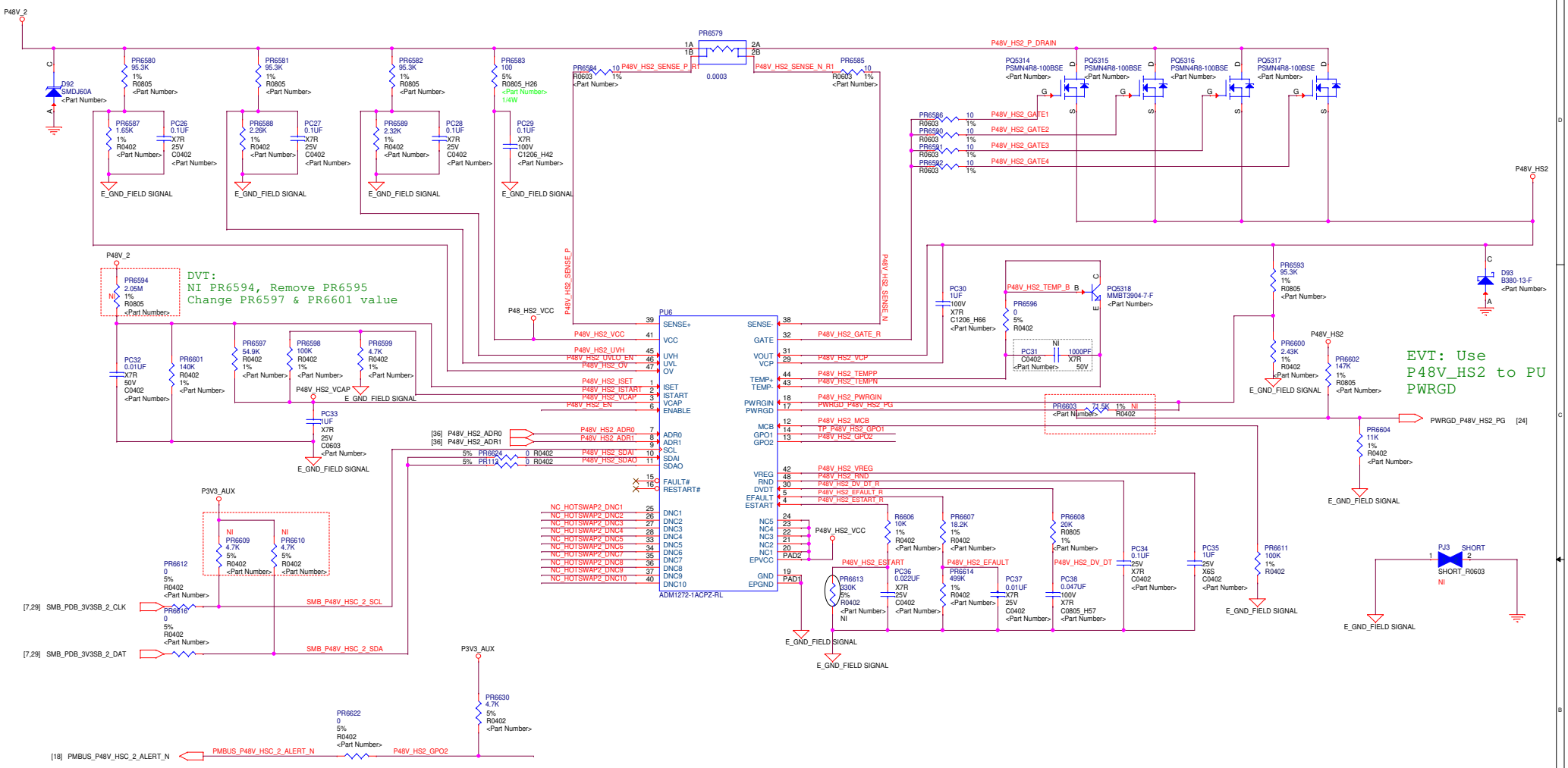
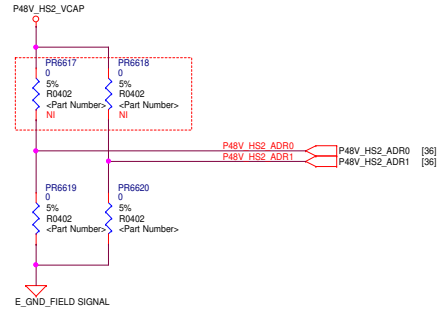


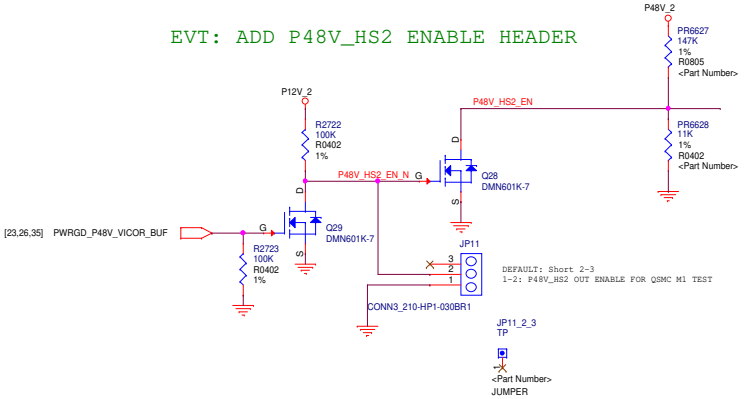
Table 9. PMBus Address Decode (7-Bit Address)

ADR2 State	ADR1 State	Device Address
Low	Low	0x10
Low	Resistor	0x11
Low	High-Z	0x12
Low	High	0x13
Resistor	Low	0x14
Resistor	Resistor	0x15
Resistor	High-Z	0x16
Resistor	High	0x17
High-Z	Low	0x18
High-Z	Resistor	0x19
High-Z	High-Z	0x1A
High-Z	High	0x1B
High	Low	0x1C
High	Resistor	0x1D
High	High-Z	0x1E
High	High	0x1F



SMB Address:0x10(7bit),0x20(8bit)
ADR0=0
ADR1=0

EVT: ADD P48V_HS2 ENABLE HEADER



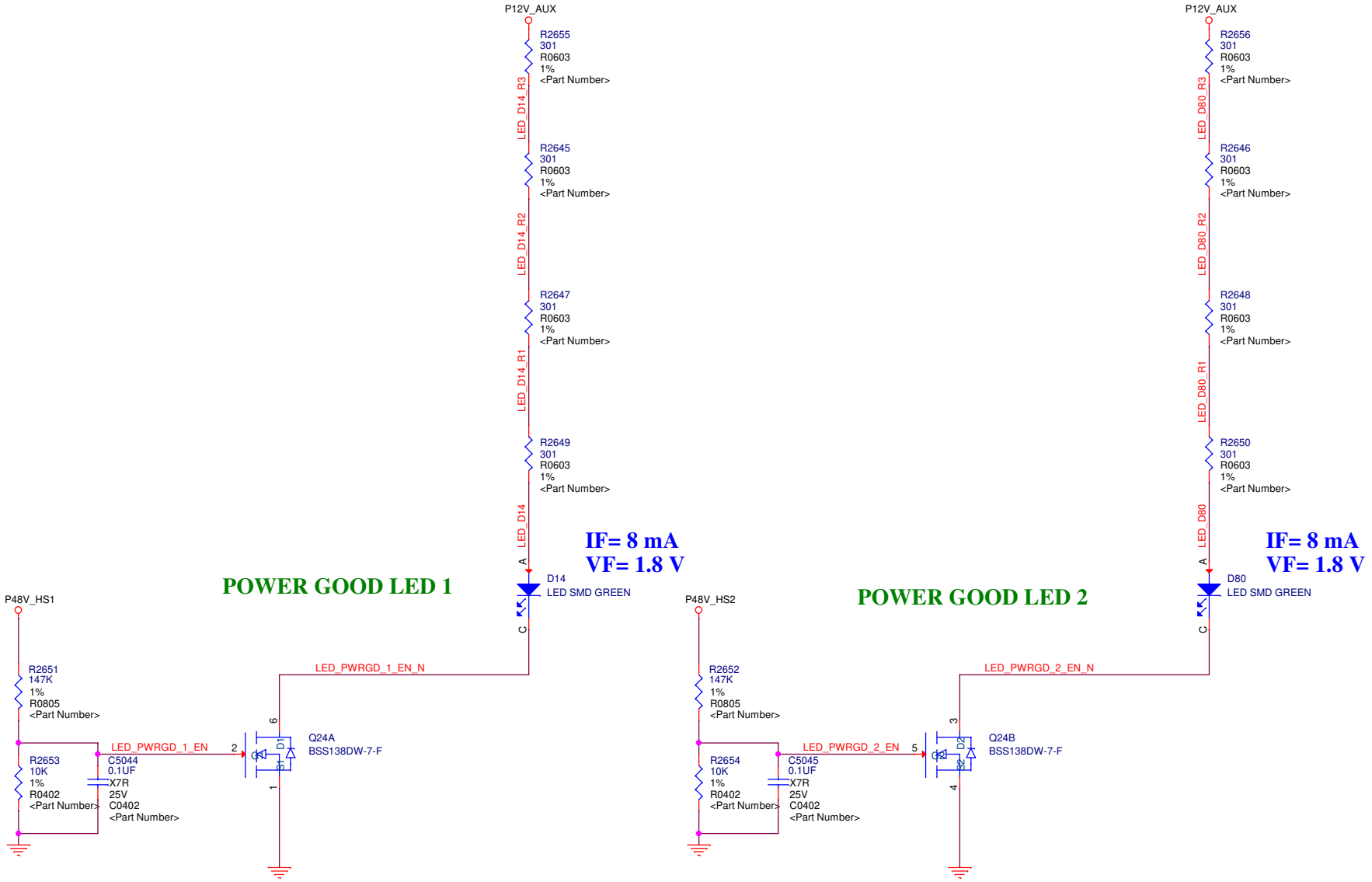
UV/OV/PG Thresholds

	min.	typical	max.
Rising UVLO	41.893	43.168	44.443
Falling UVLO	38.360	39.710	41.060
Rising OVLO	58.052	59.827	61.602
Falling OVLO	57.51	59.35	61.19
Rising PG	NA	42.12	NA
Falling PG	NA	39.74	NA

Unit: V

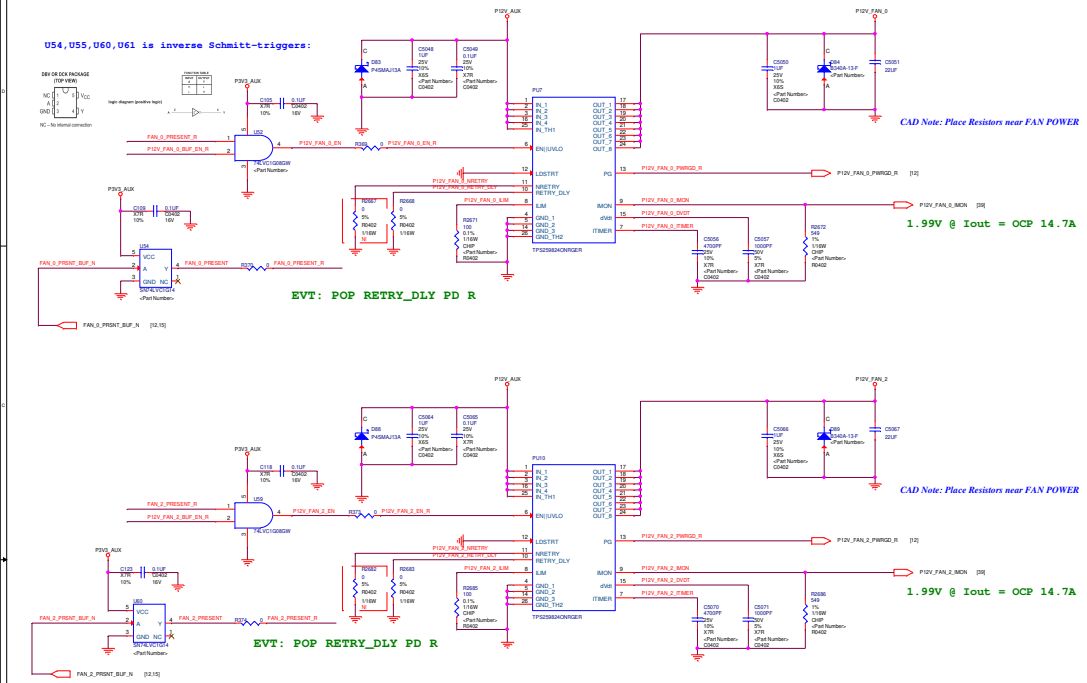
Current Limit & Circuit breaker

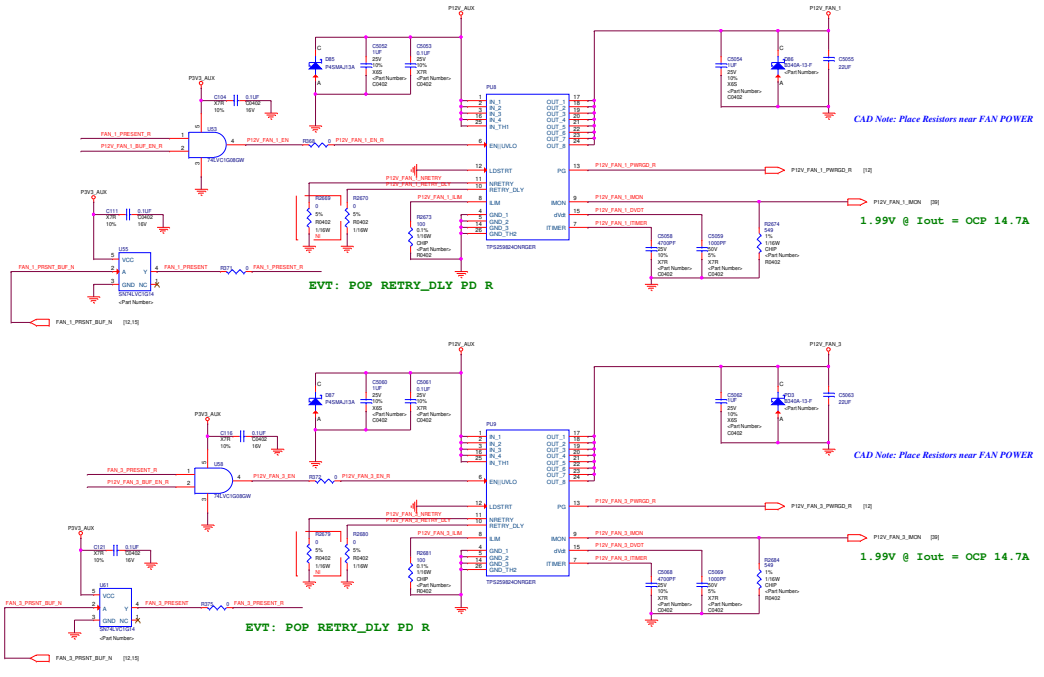
Resulting Current Limit: 3KW (63A)

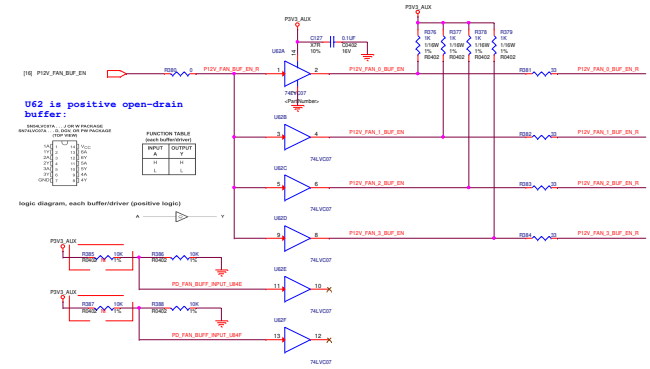


POWER GOOD LED

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EFUSE P12V_FAN

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ROUTE ALL ADC NETS AT 10 MILLS WIDE

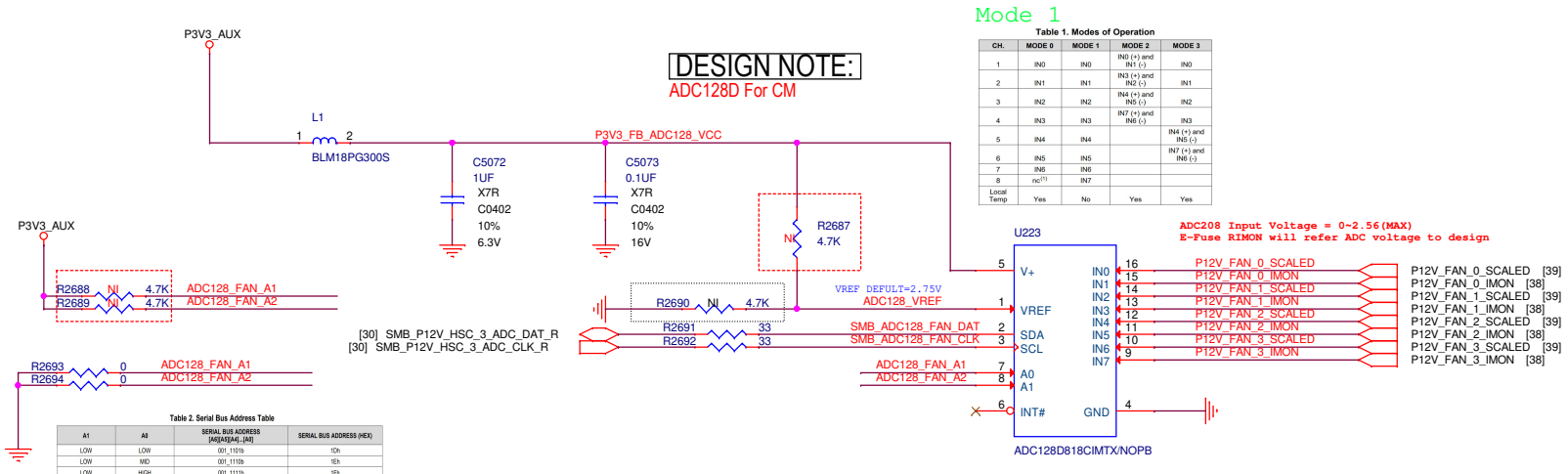


Table 1. Modes of Operation

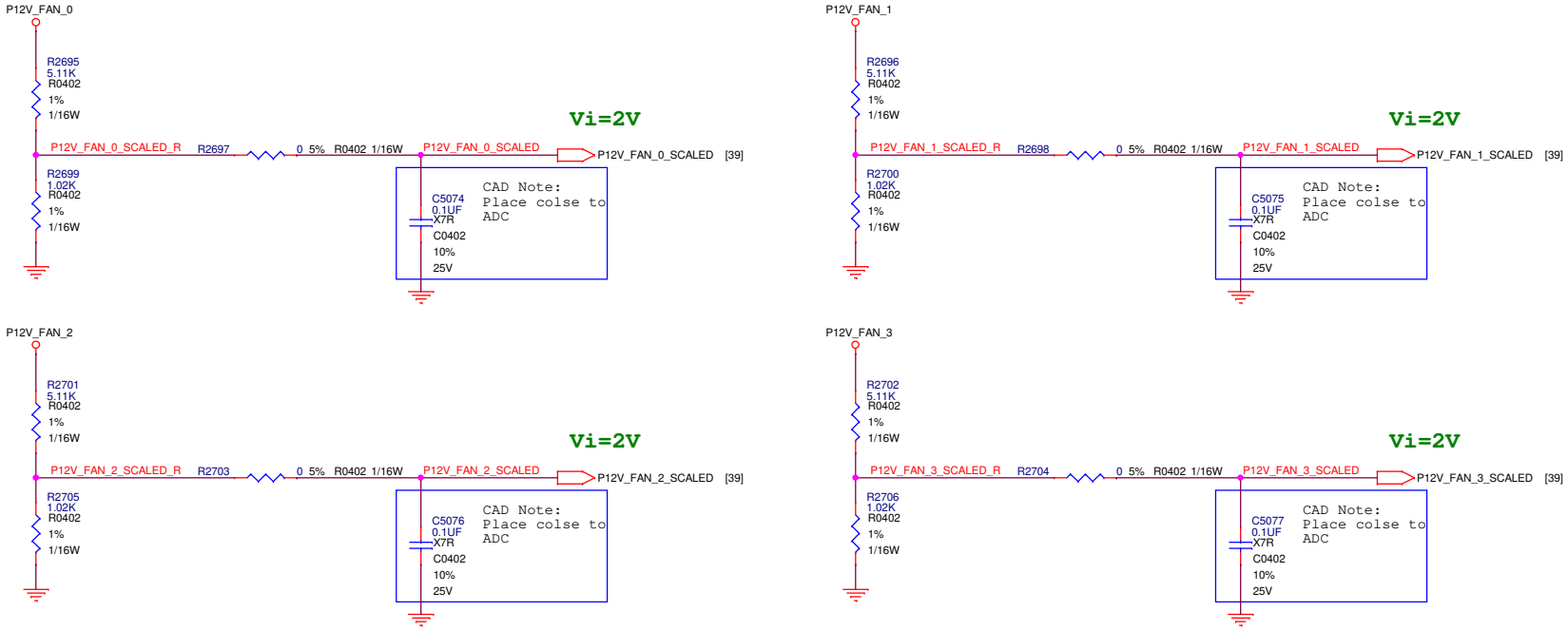
CH.	MODE 0	MODE 1	MODE 2	MODE 3
1	IN0	IN0	IN0 (+) and IN1 (-)	IN0
2	IN1	IN1	IN3 (+) and IN2 (-)	IN1
3	IN2	IN2	IN4 (+) and IN5 (-)	IN2
4	IN3	IN3	IN7 (+) and IN6 (-)	IN3
5	IN4	IN4		IN4 (+) and IN5 (-)
6	IN5	IN5		IN7 (+) and IN6 (-)
7	IN6	IN6		
8	nc[1]	IN7		
Local Temp	Yes	No	Yes	Yes

Table 2. Serial Bus Address Table

A1	A0	SERIAL BUS ADDRESS [A6][A5][A4]...[A0]	SERIAL BUS ADDRESS (HEX)
LOW	LOW	001_1101b	1Dh
LOW	MID	001_1110b	1Eh
LOW	HIGH	001_1111b	1Fh
MID	LOW	010_1101b	2Dh
MID	MID	010_1110b	2Eh
MID	HIGH	010_1111b	2Fh
HIGH	LOW	011_0101b	35h
HIGH	MID	011_0110b	36h
HIGH	HIGH	011_0111b	37h

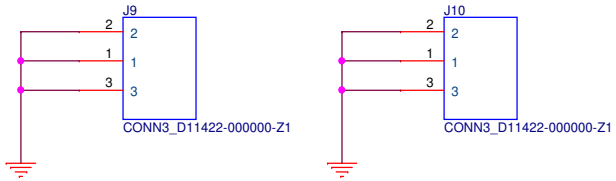
DESIGN NOTE:
SMBUS ADDERSS: 0X3A

CAD Note: Place near ADC



VOLTAGE/CURRENT MON ADC

PDB FEMALE RIGHT ANGLE GUIDE PIN



BOM NOTE : J9 J10 DIP PART

HEATSINK

HS

1

TP

<Part Number>

BRACKET

BARCKET_ASSY

1

TP

<Part Number>

ME_LABEL1

DUMMY_SYMBOL

<Part Number>

ME_LABEL2

DUMMY_SYMBOL

<Part Number>

HANDLE SCREW*4

H30_SCREW H31_SCREW H32_SCREW H33_SCREW

1 1 1 1

TP TP TP TP

<Part Number> <Part Number> <Part Number> <Part Number>

BRACKET SCREW*2

H21_SCREW H22_SCREW

1 1

TP TP

<Part Number> <Part Number>

GUIDE PIN SCREW*2

J9_SCREW J10_SCREW

1 1

TP TP

<Part Number> <Part Number>

HADLE*2

HANDLE_1 HANDLE_2

1 1

TP TP

<Part Number> <Part Number>

THUMB SCREW*4

H23_THUMB H24_THUMB H25_THUMB H26_THUMB

1 1 1 1

TP TP TP TP

<Part Number> <Part Number> <Part Number> <Part Number>

BJT_HOLDER

BJT_HOLDER

1

TP

<Part Number>

GUIDE PIN & ME PART

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GOURD SCREW HOLE

H7
HOLE_C9D3_5B9_OB5XC4-5_NPM_SPD
NI

H8
HOLE_C9D3_5B9_OB5XC4-5_NPM_SPD
NI

H9
HOLE_C9D3_5B9_OB5XC4-5_NPM_SPD
NI

H10
HOLE_C9D3_5B9_OB5XC4-5_NPM_SPD
NI

H11
HOLE_C9D3_5B9_OB5XC4-5_NPM_SPD
NI

H12
HOLE_C9D3_5B9_OB5XC4-5_NPM_SPD
NI

H13
HOLE_C9D3_5B9_OB5XC4-5_NPM_SPD
NI

H14
HOLE_C9D3_5B9_OB5XC4-5_NPM_SPD
NI

H15
HOLE_C9D3_5B9_OB5XC4-5_NPM_SPD
NI

H16
HOLE_C9D3_5B9_OB5XC4-5_NPM_SPD
NI

H17
HOLE_C9D3_5B9_OB5XC4-5_NPM_SPD
NI

H18
HOLE_C9D3_5B9_OB5XC4-5_NPM_SPD
NI

H19
HOLE_C9D3_5B9_OB5XC4-5_NPM_SPD
NI

H20
HOLE_C9D3_5B9_OB5XC4-5_NPM_SPD
NI

Heatsink SCREW HOLE

H21
GNDHOLE_8PIN
NI

H22
GNDHOLE_8PIN
NI

THUMB SCREW HOLE

H23
HOLE_C10-2D6-4B10-2_OB5XC5-1B_NPB
NI

H24
HOLE_C10-2D6-4B10-2_OB5XC5-1B_NPB
NI

H25
HOLE_C10-2D6-4B10-2_OB5XC5-1B_NPB
NI

H26
HOLE_C10-2D6-4B10-2_OB5XC5-1B_NPB
NI

Tooling Holes

H27
NI
HOLE_TOOLINGD125N_T2-0

H28
NI
HOLE_TOOLINGD125N_T2-0

H29
NI
HOLE_TOOLINGD125N_T2-0

HANDLE SCREW HOLE

H30
HOLE_C11D5-6B11_NPB
NI

H31
HOLE_C11D5-6B11_NPB
NI

H32
HOLE_C11D5-6B11_NPB
NI

H33
HOLE_C11D5-6B11_NPB
NI

SCREW HOLE

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LOSS COUPON

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PCBA_LABEL

Lable_SN_QPN_FBPN

DUMMY_SYMBOL

SNLABEL_27X6

<Part Number>

WEEE

DM3

DUMMY_SYMBOL

WEEE

NI

PB-E1

DM4

DUMMY_SYMBOL

PB-E1_SMALL

NI

BARCODE(TOP)

BARCODE(BOT)

Laser Mark(TOP)

Laser Mark(BOT)

Quanta LOGO(TOP)

DM8

DUMMY_SYMBOL

QUANTA_LOGO_7X26

NI

BMC AMI Laser label

PCB_VENDER_LOGO

DM6

DUMMY_SYMBOL

PCB_VENDOR_LOGO_15X8

NI

Dummy symbol

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